

TPS65930/TPS65920

Integrated Power Management/ Audio Codec (TPS65930 Only)

Silicon Revision 1.0

Version A

Data Manual



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1 Introduction

The TPS65920/TPS65930 devices are power-management ICs for OMAP™ and other mobile applications. The devices include power-management, a universal serial bus (USB) high-speed (HS) transceiver, LED drivers, an analog-to digital converter (ADC), a real-time clock (RTC), and embedded power control (EPC). In addition, the TPS65930 includes a full audio codec with two digital-to-analog converters (DACs) and two ADCs to implement dual voice channels, and a stereo downlink channel that can play all standard audio sample rates through a multiple format inter-integrated sound (I2S™)/time division multiplexing (TDM) interface.

These optimized devices support the power and peripheral requirements of the OMAP application processors. The power portion of the devices contains three buck converters, two controllable by a dedicated SmartReflex™ class-3 interface, multiple low dropout (LDO) regulators, an EPC to manage the power sequencing requirements of OMAP, and an RTC and backup module. The RTC can be powered by a backup battery when the main supply is not present, and the devices include a coin-cell charger to recharge the backup battery as needed.

The USB module provides a HS 2.0 OTG transceiver suitable for direct connection to the OMAP UTMI+ low pin (ULPI) interface, with an integrated charge pump and full support for the Carkit CEA0936A specification. An ADC is provided for monitoring signals, such as supply voltage, entering the device, and two additional external ADC inputs are provided for system use.

The devices provide driver circuitry to power two light-emitting diode (LED) circuits that can illuminate a panel or provide user indicators. The drivers also provide pulse width modulation (PWM) circuits to control the illumination levels of the LEDs. A keypad interface implements a built-in scanning algorithm to decode hardware-based key presses and reduce software use, with multiple additional general-purpose input/output devices (GPIOs) that can be used as interrupts when configured as inputs.

This TPS65920/TPS65930 data manual presents the electrical and mechanical specifications for the TPS65920 and TPS65930 devices. It covers the following topics:

- TPS65920/TPS65930 terminals: Assignment, multiplexing, electrical characteristics, and functional description (see [Section 2, Terminal Description](#))
- Electrical characteristic requirements: Maximum and recommended operating conditions, digital input/output (I/O) characteristics (see [Section 3, Electrical Characteristics](#))
- Power module: Power provider, power references, power control, power consumption, and power management, with the on and off sequence (see [Section 4, Power Module](#))
- RTC and EPC (see [Section 5, Real-Time Clock and Embedded Power Controller](#))
- Audio/voice module (TPS65930 device only): Electrical characteristics and application schematics for the downlink and uplink paths (see [Section 6, Audio/Voice Module \(TPS65930 Device Only\)](#))
- Various modules: USB transceiver, monitoring analog-to-digital converter (MADC), LED drivers, and keyboard (see [Section 8, MADC](#), [Section 9, LED Driver](#), and [Section 10, Keyboard](#))
- Clock specifications: Clock slicer; input and output clocks (see [Section 11, Clock Specifications](#))
- Timing requirements and switching characteristics (ac timings) of the interfaces (see [Section 12, Timing Requirements and Switching Characteristics](#))
- Debouncing time (see [Section 13, Debouncing Time](#))
- External components for the application schematics (see [Section 14, External Components](#))
- Thermal resistance characteristics, device nomenclature, and mechanical data about the available packaging (see [Section 15, TPS65920/TPS65930 Package](#))
- Glossary of acronyms and abbreviations used in this data manual (see [Section 16, Glossary](#))



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1.1 Features

The TPS65930 and TPS65920 devices offer the following features:

- **Power:**
 - Three efficient stepdown converters
 - Four external linear LDOs for clocks and peripherals
 - SmartReflex™ dynamic voltage management
- Audio (TPS65930 device only):
 - Differential input main microphones
 - Mono auxiliary/FM input
 - External predrivers for class D (stereo)
 - Time division multiplexing (TDM) interface
 - Automatic level control (ALC)
 - Digital and analog mixing
 - 16-bit linear audio stereo digital-to-analog converter (DAC) (96, 48, 44.1, and 32 kHz and derivatives)
 - 16-bit linear audio stereo analog-to-digital converter (ADC) (48, 44.1, and 32 kHz and derivatives)
 - Carkit
- Universal serial bus (USB):
 - USB 2.0 on-the-go (OTG)-compliant high-speed (HS) transceivers
 - 12-bit universal transceiver macro interface (UTMI) + low pin interface (ULPI)
 - USB power supply (5-V charge pump for VBUS)
 - Consumer Electronics Association (CEA)-2011: OTG transceiver interface specification
 - CEA-936A: Mini-USB analog carkit specification
- Additional Features:
 - LED driver circuit for two external LEDs
 - Two external 10-bit MADC inputs
 - Real-time clock (RTC) and retention modules
 - HS inter-IC sound (I2S™) serial control
 - Thermal shutdown and hot-die detection
 - Keypad Interface (up to 6 × 6)
 - External vibrator control
 - 15 general-purpose input/outputs (GPIOs)
 - 0.65 mm pitch, 139 pin, 10 × 10 mm package

1.1 TPS65920 and TPS65930 Device Block Diagrams

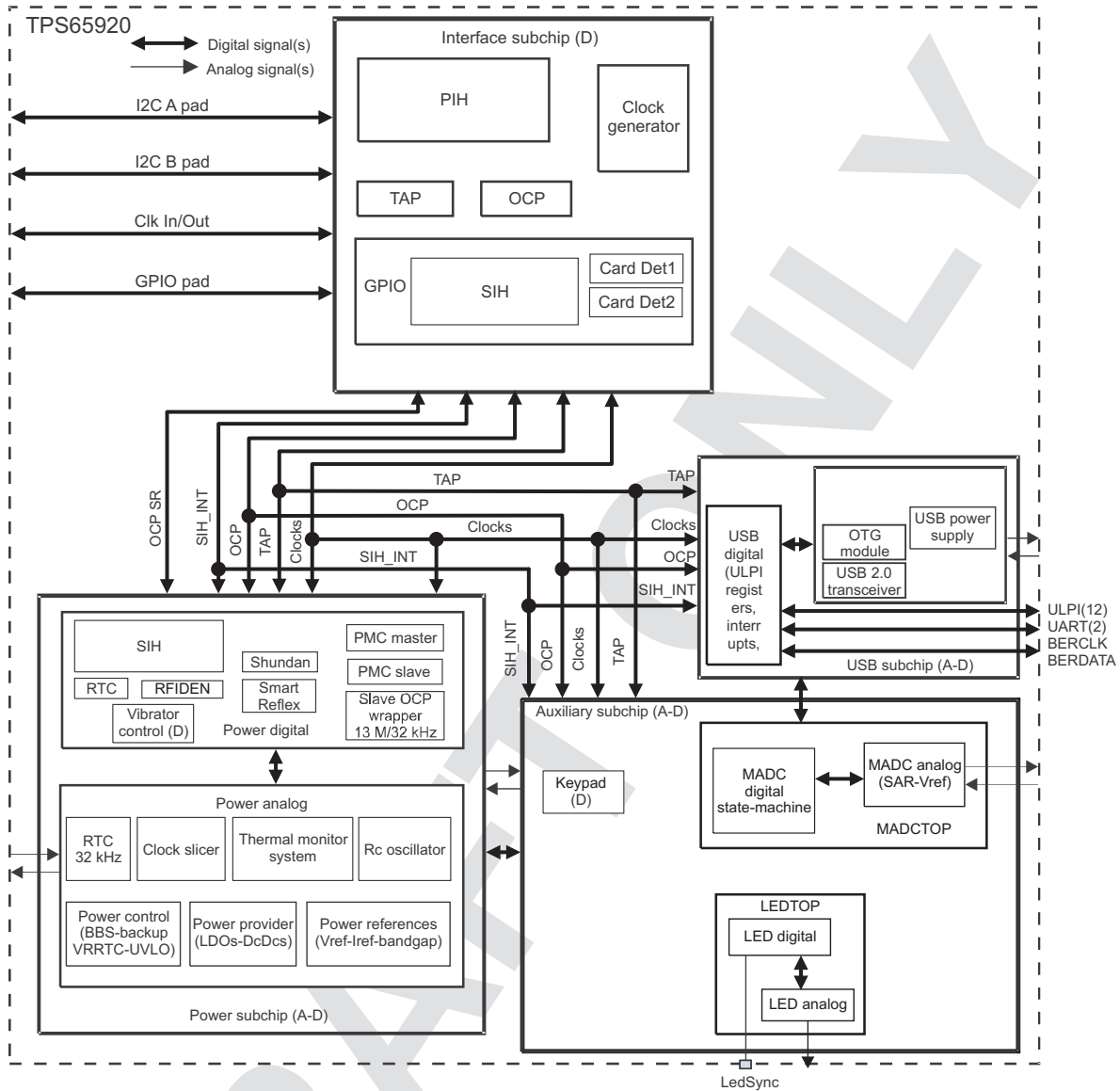


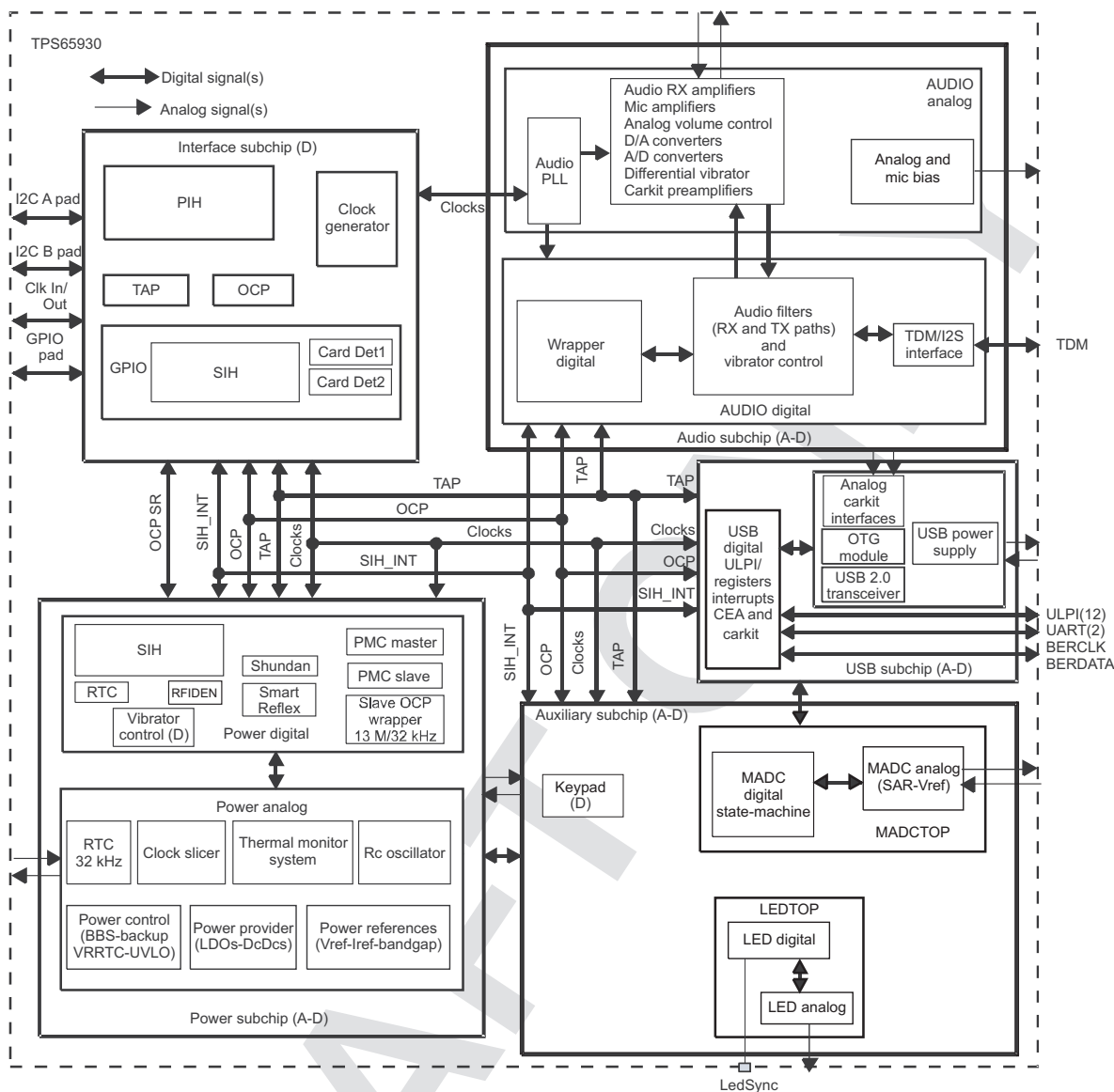
Figure 1-1. TPS65920 Block Diagram

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Figure 1-2. TPS65930 Block Diagram

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Table 2-1. Ball Characteristics (continued)

TPS65920 Ball[1]	TPS65930 Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (k Ω)			PD[6] (k Ω)			Buffer Strength (mA)[7]
						Min	Typ	Max	Min	Typ	Max	
P2	P2	GPIO.2	D	I/O	IO_1P8	156	220	450	59	100	144	2
		TEST1	D	I/O	IO_1P8							2
P13	P13	GPIO.15	D	I/O	IO_1P8	156	220	450	59	100	144	2
		TEST2	D	I/O	IO_1P8							2
L5	L5	GPIO.6	D	I/O	IO_1P8	75	100	202	59	100	144	2
		PWM0	D	O	IO_1P8							4
		TEST3	D	I/O	IO_1P8							2
J7	J7	GPIO.7	D	I/O	IO_1P8	75	100	202	59	100	144	2
		VIBRA.SYNC	D	I	IO_1P8							
		PWM1	D	O	IO_1P8							4
		TEST4	D	I/O	IO_1P8							2
D8	D8	SYSEN	D	Open drain/I	IO_1P8	4.7	7.35	10				2
A4	A4	CLKEN	D	O	IO_1P8							2
B13	B13	CLKREQ	D	I	IO_1P8				60	100	146	
C10	C10	INT1	D	O	IO_1P8							2
C8	C8	NRESPWRON	D	O	IO_1P8							2
B9	B9	NRESWARM	D	I	IO_1P8							2
D10	D10	PWRON	D	I	VBAT							
G5	G5	NSLEEP1	D	I	IO_1P8							
E10	E10	CLK256FS ⁽¹⁾	D	O	IO_1P8							2
E4	E4	VMODE1	D	I	IO_1P8							
E8	E8	BOOT0	A/D	I/O	VBAT							
D7	D7	BOOT1	A/D	I/O	VBAT							
B8	B8	REGEN	D	Open drain	VBAT	5.5	8	12				2
H4	H4	MSECURE	D	I	IO_1P8							
L13	L13	VREF	A	Power	VREF							
K13	K13	AGND	A	Power ground (GND)	GND							
B3	B3	N.C.										
		I2C.SR.SDA	D	I/O	IO_1P8	2.5		3.4				12
C5	C5	VMODE2	D	I	IO_1P8							2
		I2C.SR.SCL	D	I/O	IO_1P8	2.5		3.4				12
C3	C3	I2C.CNTL.SDA	D	I/O	IO_1P8	2.5		3.4				12
B4	B4	I2C.CNTL.SCL	D	I	IO_1P8	2.5		3.4				12
	H3	I2S.CLK	D	I/O	IO_1P8							2
	K2	I2S.SYNC	D	I/O	IO_1P8							2
	K4	I2S.DIN	D	I	IO_1P8							2
	K3	I2S.DOUT	D	O	IO_1P8							2
	D1	MIC.MAIN.P	A	I	MICBIAS1.OUT							
	E1	MIC.MAIN.M	A	I	MICBIAS1.OUT							
A10	A10	VBAT.RIGHT	A	Power	VBAT							
	A7	PreDrv.LEFT	A	O	VINTANA2.OUT							
		VMID	A	Power	VINTANA2.OUT							
	A8	PreDrv.RIGHT	A	O	VINTANA2.OUT							
		ADCIN7	A	I	VINTANA2.OUT							
	G1	AUXR	A	I	VINTANA2.OUT							
	E2	MICBIAS1.OUT	A	Power	VINTANA2.OUT							
		VMIC1.OUT	A	Power	VINTANA2.OUT							
	D2	MICBIAS.GND		Power GND	GND							
G2	G2	AVSS1	A	Power GND	GND							
L7	L7	AVSS2	A	Power GND	GND							
N14	N14	AVSS3	A	Power GND	GND							
C7	C7	AVSS4	A	Power GND	GND							

(1) To avoid reflection on this pin as a result of impedance mismatch, a serial resistance of 33 Ω must be added.

Table 2-1. Ball Characteristics (continued)

TPS65920 Ball[1]	TPS65930 Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (k Ω)			PD[6] (k Ω)			Buffer Strength (mA)[7]
						Min	Typ	Max	Min	Typ	Max	
M10	M10	32KCLKOUT	D	O	IO_1P8							
L14	L14	32KXIN	A	I	IO_1P8							
K14	K14	32KXOUT	A	O	IO_1P8							
A11	A11	HFCLKIN	A	I	IO_1P8							
M11	M11	HFCLKOUT	D	O	IO_1P8							
P8	P8	VBUS	A	Power	VBUS							
N10	N10	DP/UART3.RXD	A	I/O	VBUS							2
P10	P10	DN/UART3.TXD	A	I/O	VBUS							2
G6	G6	ID	A	I/O	VBUS							2
K11	K11	UCLK	D	I/O	IO_1P8							16
H12	H12	STP	D	I	IO_1P8	75	100	202	59	100	144	16
		GPIO.9	D	I/O	IO_1P8							2
H11	H11	DIR	D	O	IO_1P8	75	100	202	59	100	144	16
		GPIO.10	D	I/O	IO_1P8							2
J8	J8	NXT	D	O	IO_1P8	75	100	202	59	100	144	16
		GPIO.11	D	I/O	IO_1P8							2
L10	L10	DATA0	D	I/O	IO_1P8							16
		UART4.TXD	D	I	IO_1P8							
K10	K10	DATA1	D	I/O	IO_1P8							16
		UART4.RXD	D	O	IO_1P8							2
G11	G11	DATA2	D	I/O	IO_1P8							16
		UART4.RTSI	D	I	IO_1P8							
G10	G10	DATA3	D	I/O	IO_1P8	60	100	140	60	100	140	16
		UART4.CTSO	D	O	IO_1P8							16
		GPIO.12	D	I/O	IO_1P8	75	100	202	59	100	144	16
E12	E12	DATA4	D	I/O	IO_1P8	75	100	202	59	100	144	16
		GPIO.14	D	I/O	IO_1P8							2
G9	G9	DATA5	D	I/O	IO_1P8	75	100	202	59	100	144	16
		GPIO.3	D	I/O	IO_1P8							2
G12	G12	DATA6	D	I/O	IO_1P8	75	100	202	59	100	144	16
		GPIO.4	D	I/O	IO_1P8							2
E11	E11	DATA7	D	I/O	IO_1P8	75	100	202	59	100	144	16
		GPIO.5	D	I/O	IO_1P8							2
P14	P14	TEST.RESET	A/D	I	VBAT				30	50	70	
P1	P1	TESTV1	A	I/O	VBAT							
A14	A14	TESTV2	A	I/O	VINTANA2.OUT							
A1	A1	TEST	D	I	IO_1P8				60	100	146	
A13	A13	JTAG.TDI/ BERDATA	D	I	IO_1P8							
B14	B14	JTAG.TCK/ BERCLK	D	I	IO_1P8							
P7	P7	CP.IN	A	Power	VBAT/VBUS							
N7	N7	CP.CAPP	A	O	CP.CAPP							
N6	N6	CP.CAPM	A	O	CP.CAPM							
P5	P5	CP.GND	A	Power GND	GND							
N9	N9	VBAT.USB	A	Power	VBAT							
M8	M8	VUSB.3P1	A	Power	VUSB.3P1							
L1	L1	VAUX12S.IN	A	Power	VBAT							
N2	N2	VAUX2.OUT	A	Power	VAUX2.OUT							
H14	H14	VPLLA3R.IN	A	Power	VBAT							
K12	K12	VRTC.OUT	A	Power	VRTC.OUT							
G14	G14	VPLL1.OUT	A	Power	VPLL1.OUT							
A2	A2	VMMC1.IN	A	Power	VBAT							
B1	B1	VMMC1.OUT	A	Power	VMMC1.OUT							

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Table 2-1. Ball Characteristics (continued)

TPS65920 Ball[1]	TPS65930 Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (k Ω)			PD[6] (k Ω)			Buffer Strength (mA)[7]
						Min	Typ	Max	Min	Typ	Max	
M7	M7	VINTUSB1P5. OUT	A	Power	VINTUSB1P5.OUT							
N8	N8	VINTUSB1P8. OUT	A	Power	VINTUSB1P8.OUT							
K1	K1	VDAC.IN	A	Power	VBAT							
L2	L2	VDAC.OUT	A	Power	VDAC.OUT							
H13	H13	VINT.IN	A	Power	VBAT							
H1	H1	VINTANA1.OUT	A	Power	VINTANA1.OUT							
J2	J2	VINTANA2.OUT	A	Power	VINTANA2.OUT							
A5	A5	VINTANA2.OUT	A	Power	VINTANA2.OUT							
J13	J13	VINTDIG.OUT	A	Power	VINTDIG.OUT							
D13	D13	VDD1.IN	A	Power	VBAT							
D12	D12	VDD1.IN	A	Power	VBAT							
D14	D14	VDD1.IN	A	Power	VBAT							
C11	C11	VDD1.SW	A	O	VBAT							
C12	C12	VDD1.SW	A	O	VBAT							
C13	C13	VDD1.SW	A	O	VBAT							
E14	E14	VDD1.FB	A	I								
A12	A12	VDD1.GND	A	Power GND	GND							
B11	B11	VDD1.GND	A	Power GND	GND							
B12	B12	VDD1.GND	A	Power GND	GND							
M13	M13	VDD2.IN	A	Power	VBAT							
M12	M12	VDD2.IN	A	Power	VBAT							
N13	N13	VDD2.FB	A	I								
N11	N11	VDD2.SW	A	O	VBAT							
P11	P11	VDD2.SW	A	O	VBAT							
N12	N12	VDD2.GND	A	Power GND	GND							
P12	P12	VDD2.GND	A	Power GND	GND							
M2	M2	VIO.IN	A	Power	VBAT							
M3	M3	VIO.IN	A	Power	VBAT							
M4	M4	VIO.FB	A	I								
N4	N4	VIO.SW	A	O	VBAT							
P4	P4	VIO.SW	A	O	VBAT							
N3	N3	VIO.GND	A	Power GND	GND							
P3	P3	VIO.GND	A	Power GND	GND							
H9	H9	BKBAT	A	Power	VBACK							
B7	B7	IO_1P8	A	Power	IO_1P8							
H10	H10	DGND	A	Power GND	GND							
F13	F13	LEDGND	A	Power GND	GND							
B10	B10	GPIO.13	D	I/O	IO_1P8	75	100	202	59	100	144	
		LEDSYNC	D	I	IO_1P8							
E13	E13	LEDA	A	Open drain	VBAT							
		VIBRA.P	A	Open drain	VBAT							
G13	G13	LEDB	A	Open drain	VBAT							
		VIBRA.M	A	Open drain	VBAT							
G4	G4	KPD.C0	D	Open drain	IO_1P8							
G3	G3	KPD.C1	D	Open drain	IO_1P8							
E5	E5	KPD.C2	D	Open drain	IO_1P8							
B2	B2	KPD.C3	D	Open drain	IO_1P8							
E3	E3	KPD.C4	D	Open drain	IO_1P8							
D5	D5	KPD.C5	D	Open drain	IO_1P8							
K7	K7	KPD.R0	D	I	IO_1P8	8	10	12				
H5	H5	KPD.R1	D	I	IO_1P8	8	10	12				
K5	K5	KPD.R2	D	I	IO_1P8	8	10	12				
H6	H6	KPD.R3	D	I	IO_1P8	8	10	12				

Table 2-1. Ball Characteristics (continued)

TPS65920 Ball[1]	TPS65930 Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (k Ω)			PD[6] (k Ω)			Buffer Strength (mA)[7]
						Min	Typ	Max	Min	Typ	Max	
K8	K8	KPD.R4	D	I	IO_1P8	8	10	12				
L8	L8	KPD.R5	D	I	IO_1P8	8	10	12				

2.2 Signal Description

Table 2-2 describes the signals on the TPS65920 and TPS65930 devices; some signals are available on multiple pins.

Table 2-2. Signal Description

Module	Signal Name	Description	Type	TPS65920 Ball	TPS65930 Ball	Default Configuration After Reset Released			Features Not Used ⁽¹⁾
						Signal	Type	Internal Pull or Not	
ADC	ADCIN0	Battery type	I/O	H2	H2	ADCIN0			GND
	ADCIN2	General-purpose ADC input	I	F2	F2	ADCIN2	I		GND
Charger	PCHGAC	AC precharge sense signal. Also used for EEPROM.	I	M5	M5	PCHGAC	I		GND
	VPRECH	Precharge regulator output	O	N1	N1	VPRECH	O		Cap to GND ⁽²⁾
	VBAT	Battery voltage sensing	Power	N5	N5	VBAT	Power		VBAT
GPIOs/ JTAG	GPIO.0/CD1	GPIO0/card detection 1	I/O	F7	F7	GPIO.0	I	PD	Floating
	JTAG.TDO	JTAG test data output	I/O						
	GPIO.1/CD2	GPIO1/card detection 2	I/O	E7	E7	GPIO.1	I	PD	Floating
	JTAG.TMS	JTAG test mode state	I						
	GPIO.2	GPIO2	I/O	P2	P2	GPIO.2	I	PD	Floating
	TEST1	TEST1 pin used in test mode only	I/O						
	GPIO.15	GPIO15	I/O	P13	P13	GPIO.15	I	PD	Floating
	TEST2	TEST2 pin used in test mode only	I/O						
	GPIO.6	GPIO6	I/O	L5	L5	GPIO.6	I	PD	Floating
	PWM0	Pulse width driver 0	O						
	TEST3	TEST3 pin used in test mode only (controlled by JTAG)	I/O	J7	J7	GPIO.7	I	PD	Floating
	GPIO.7	GPIO.7	I/O						
	VIBRA.SYNC	Vibrator on-off synchronization	I						
	PWM1	Pulse width driver	O						
	TEST4	TEST4 pin used in test mode only (controlled by JTAG)	I/O						

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Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type	TPS65920 Ball	TPS65930 Ball	Default Configuration After Reset Released			Features Not Used ⁽¹⁾
						Signal	Type	Internal Pull or Not	
CONTROL	SYSEN	System enable output	Open drain/I	D8	D8	SYSEN	OD	PU	Floating
	CLKEN	Clock enable	O	A4	A4	CLKEN	O		Floating
	CLKREQ	Clock request	I	B13	B13	CLKREQ	I	PD	GND
	INT1	Output interrupt line 1	O	C10	C10	INT1	O		Floating
	NRESPWRON	Output control the NRESPWRON of the application processor	O	C8	C8	NRESPWRON	O		Floating
	NRESWARM	Input; detect user action on the reset button	I	B9	B9	NRESWARM	I		GND
	PWRON	Input; detect a control command to start or stop the system	I	D10	D10	PWRON	I		VBAT
	NSLEEP1	Sleep request from device 1	I	G5	G5	NSLEEP1	I		GND
	CLK256FS		O	E10	E10	CLK256FS	O		Floating
	VMODE1	Digital voltage scaling linked with VDD1	I	E4	E4	VMODE1	I		GND
	BOOT0	Boot pin 0	I	E8	E8	BOOT0	I	PD	N/A
	BOOT1	Boot pin 1	I	D7	D7	BOOT1	I	PD	N/A
	REGEN	Enable signal for external LDO	Open drain	B8	B8	REGEN	OD	PU	Floating
	MSECURE	Security and digital rights management	I	H4	H4	MSECURE	I		N/A
VREF	VREF	Reference voltage	Power	L13	L13	VREF	Power		N/A
	AGND	Analog ground for reference voltage	Power GND	K13	K13	AGND	Power GND		GND
I ² C Smart Reflex	N.C.	Not connected		B3	B3	Signal not functional ⁽³⁾			Floating
	I2C.SR.SDA	SmartReflex I ² C data	I/O						
	VMODE2	Digital voltage scaling linked with VDD2	I	C5	C5	VMODE2	I		GND
	I2C.SR.SCL	SmartReflex I ² C data	I/O						
I ² C	I2C.CNTL.SDA	General-purpose I ² C data	I/O	C3	C3	I2C.CNTL.SDA	I/O	PU	N/A
	I2C.CNTL.SCL	General-purpose I ² C clock	I/O	B4	B4	I2C.CNTL.SCL	I/O	PU	N/A
TDM	I2S.CLK	Clock signal (audio port)	I/O		H3	I2S.CLK	I/O		Floating
	I2S.SYNC	Synchronization signal (audio port)	I/O		K2	I2S.SYNC	I/O		Floating
	I2S.DIN	Data receive (audio port)	I		K4	I2S.DIN	I		GND
	I2S.DOUT	Data transmit (audio port)	O		K3	I2S.DOUT	O		Floating
ANA.MIC	MIC.MAIN.P	Main microphone left input (P)	I		D1	MIC.MAIN.P	I		Cap to GND
	MIC.MAIN.M	Main microphone left input (M)	I		E1	MIC.MAIN.M	I		Cap to GND
Hands-Free	VBAT.RIGHT	Battery voltage input	Power	A10	A10	VBAT.RIGHT	Power		VBAT
Headset	PreDrv.LEFT	Predriver output left P for external class-D amplifier	O		A7	VMID	Power		Floating
	VMID		Power						
	PreDrv.RIGHT	Predriver output right P for external class-D amplifier	O		A8	ADCIN7	I		GND
	ADCIN7	General-purpose ADC input 7	I						
AUX Input	AUXR	Auxiliary audio input right	I		G1	AUXR	I		Cap to GND

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type	TPS65920 Ball	TPS65930 Ball	Default Configuration After Reset Released			Features Not Used ⁽¹⁾
						Signal	Type	Internal Pull or Not	
VMIC BIAS	MICBIAS1.OUT	Analog microphone bias 1	Power		E2	MICBIAS1.OUT	Power		Floating
	VMIC1.OUT	Digital microphone power supply 1	Power						
	MICBIAS.GND	Dedicated ground for microphones	Power GND		D2	MICBIAS.GND	Power GND		GND
	AVSS1	Analog ground	Power GND	G2	G2	AVSS1	Power GND		GND
	AVSS2			L7	L7	AVSS2			
	AVSS3			N14	N14	AVSS3			
	AVSS4			C7	C7	AVSS4			
CLOCK	32KCLKOUT	Buffered output of the 32-kHz digital clock	O	M10	M10	32KCLKOUT	O		Floating
	32KXIN	Input of the 32-kHz oscillator	I	L14	L14	32KXIN	I		N/A
	32KXOUT	Output of the 32-kHz oscillator	O	K14	K14	32KXOUT	O		Floating
	HFCLKIN	Input of the digital (or sine) HS clock	I	A11	A11	HFCLKIN	I		N/A
	HFCLKOUT	HS clock output	O	M11	M11	HFCLKOUT	O		Floating
USB PHY	VBUS	VBUS power rail	Power	P8	P8	VBUS	Power		N/A
	DP/UART3.RXD	USB data P/USB carkit receive data/universal asynchronous receiver/transmitter (UART)3 receive data	I/O	N10	N10	DP/UART3.RXD	I/O		N/A
	DN/UART3.TXD	USB data N/USB carkit transmit data/UART3 transmit data	I/O	P10	P10	DN/UART3.TXD	I/O		N/A
	ID	USB ID	I/O	G6	G6	ID	I/O		Connected to VRUSB3V1
ULPI	UCLK	HS USB clock	I/O	K11	K11	UCLK	O		Floating
	STP	HS USB stop	I	H12	H12	STP	I	PU	Floating
	GPIO.9	GPIO9	I/O						
	DIR	HS USB direction	O	H11	H11	DIR	O		Floating
	GPIO.10	GPIO10	I/O						
	NXT	HS USB next	O	J8	J8	NXT	O		Floating
	GPIO.11	GPIO11	I/O						
	DATA0	HS USB Data0	I/O	L10	L10	DATA0	O		Floating
	UART4.TXD	UART4.TXD	I						
	DATA1	HS USB Data1	I/O	K10	K10	DATA1	O		Floating
	UART4.RXD	UART4.RXD	O						
	DATA2	HS USB Data2	I/O	G11	G11	DATA2	O		Floating
	UART4.RTSI	UART4.RTSI	I						
	DATA3	HS USB Data3	I/O	G10	G10	DATA3	O		Floating
	UART4.CTSO	UART4.CTSO	O						
	GPIO.12	GPIO12	I/O	E12	E12	DATA4	O		Floating
	DATA4	HS USB Data4	I/O						
	GPIO.14	GPIO14	I/O	G9	G9	DATA5	O		Floating
	DATA5	HS USB Data5	I/O						
	GPIO.3	GPIO3	I/O	G12	G12	DATA6	O		Floating
	DATA6	HS USB Data6	I/O						
	GPIO.4	GPIO4	I/O	E11	E11	DATA7	O		Floating
	DATA7	HS USB Data7	I/O						
	GPIO.5	GPIO5	I/O						

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Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type	TPS65920 Ball	TPS65930 Ball	Default Configuration After Reset Released			Features Not Used ⁽¹⁾
						Signal	Type	Internal Pull or Not	
TEST	TEST.RESET	Reset T2 device (except power state-machine)	I	P14	P14	TEST.RESET	I	PD	GND
	TESTV1	Analog test	I/O	P1	P1	TESTV1	I/O		Floating
	TESTV2	Analog test	I/O	A14	A14	TESTV2	I/O		Floating
	TEST	Selection between JTAG mode and application mode for JTAG/GPIOs (with PU or PD)	I	A1	A1	TEST	I	PD	Floating
	JTAG.TDI/BERDATA	JTAG.TDI/BERDATA	I	A13	A13	JTAG.TDI/BERDATA	I		GND
	JTAG.TCK/BERCLK	JTAG.TCK/BERCLK	I	B14	B14	JTAG.TCK/BERCLK	I		GND
USB CP	CP.IN	Charge pump input voltage	Power	P7	P7	CP.IN	Power		VBAT
	CP.CAPP	Charge pump flying capacitor P	O	N7	N7	CP.CAPP	O		Floating
	CP.CAPM	Charge pump flying capacitor M	O	N6	N6	CP.CAPM	O		Floating
	CP.GND	Charge pump ground	Power GND	P5	P5	CP.GND	Power GND		GND
VBAT.USB	VBAT.USB	USB LDOs (VINTUSB1P5, VINTUSB1P8, VUSB.3P1) VBAT	Power	N9	N9	VBAT.USB	Power		VBAT
USB.LDO	VUSB.3P1	USB LDO output	Power	M8	M8	VUSB.3P1	Power		N/A
VAUX1	VAUX12S.IN	VAUX1/VAUX2/VSIM LDO input voltage	Power	L1	L1	VAUX12S.IN	Power		VBAT
VAUX2	VAUX2.OUT	VAUX2 LDO output voltage	Power	N2	N2	VAUX2.OUT	Power		Floating
VPLLA3R	VPLLA3R.IN	Input for VPLL1, VPLL2, VAUX3, and VRTC LDOs	Power	H14	H14	VPLLA3R.IN	Power		VBAT
VRTC	VRTC.OUT	VRTC internal LDO output (internal use only)	Power	K12	K12	VRTC.OUT	Power		N/A
VPLL1	VPLL1.OUT	LDO output voltage	Power	G14	G14	VPLL1.OUT	Power		Floating
VMMC1	VMMC1.IN	VMMC1 LDO input voltage	Power	A2	A2	VMMC1.IN	Power		VBAT
	VMMC1.OUT	VMMC1 LDO output voltage	Power	B1	B1	VMMC1.OUT	Power		Floating
VINTUSB1 P5	VINTUSB1P5. OUT	VINTUSB1P5 internal LDO output (internal use only)	Power	M7	M7	VINTUSB1P5. OUT	Power		Floating
VINTUSB1 P8	VINTUSB1P8. OUT	VINTUSB1P8 internal LDO output (internal use only)	Power	N8	N8	VINTUSB1P8. OUT	Power		Floating
Video DAC	VDAC.IN	Input for VDAC, VINTANA1, and VINTANA2 LDOs	Power	K1	K1	VDAC.IN	Power		VBAT
	VDAC.OUT	Output voltage of the regulator	Power	L2	L2	VDAC.OUT	Power		Floating
VINT	VINT.IN	Input for VINTDIG LDO	Power	H13	H13	VINT.IN	Power		VBAT
VINTANA1	VINTANA1. OUT	VINTANA1 internal LDO output (internal use only)	Power	H1	H1	VINTANA1. OUT	Power		N/A
VINTANA2	VINTANA2. OUT	VINTANA2 internal LDO output (internal use only)	Power	J2	J2	VINTANA2. OUT	Power		N/A
	VINTANA2. OUT	VINTANA2 internal LDO output (internal use only)	Power	A5	A5	VINTANA2. OUT	Power		N/A
VINTDIG	VINTDIG.OUT	VINTDIG internal LDO output (internal use only)	Power	J13	J13	VINTDIG.OUT	Power		N/A

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type	TPS65920 Ball	TPS65930 Ball	Default Configuration After Reset Released			Features Not Used ⁽¹⁾
						Signal	Type	Internal Pull or Not	
VDD1	VDD1.IN	VDD1 dc-dc input voltage	Power	D13	D13	VDD1.IN	Power		VBAT
	VDD1.IN	VDD1 dc-dc input voltage	Power	D12	D12	VDD1.IN	Power		VBAT
	VDD1.IN	VDD1 dc-dc input voltage	Power	D14	D14	VDD1.IN	Power		VBAT
	VDD1.SW	VDD1 dc-dc switch	O	C11	C11	VDD1.SW	O		Floating
	VDD1.SW	VDD1 dc-dc switch	O	C12	C12	VDD1.SW	O		Floating
	VDD1.SW	VDD1 dc-dc switch	O	C13	C13	VDD1.SW	O		Floating
	VDD1.FB	VDD1 dc-dc output voltage (feedback)	I	E14	E14	VDD1.FB	I		GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	A12	A12	VDD1.GND	Power GND		GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	B11	B11	VDD1.GND	Power GND		GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	B12	B12	VDD1.GND	Power GND		GND
VDD2	VDD2.IN	VDD2 dc-dc input voltage	Power	M13	M13	VDD2.IN	Power		VBAT
	VDD2.IN	VDD2 dc-dc input voltage	Power	M12	M12	VDD2.IN	Power		VBAT
	VDD2.FB	VDD2 dc-dc output voltage (feedback)	I	N13	N13	VDD2.FB	I		GND
	VDD2.SW	VDD2 dc-dc switch	O	N11	N11	VDD2.SW	O		Floating
	VDD2.SW	VDD2 dc-dc switch	O	P11	P11	VDD2.SW	O		Floating
	VDD2.GND	VDD2 dc-dc ground	Power GND	N12	N12	VDD2.GND	Power GND		GND
VIO	VDD2.GND	VDD2 dc-dc ground	Power GND	P12	P12	VDD2.GND	Power GND		GND
	VIO.IN	VIO dc-dc input voltage	Power	M2	M2	VIO.IN	Power		VBAT
	VIO.IN	VIO dc-dc input voltage	Power	M3	M3	VIO.IN	Power		VBAT
	VIO.FB	VIO dc-dc output voltage (feedback)	I	M4	M4	VIO.FB	I		GND
	VIO.SW	VIO dc-dc switch	O	N4	N4	VIO.SW	O		Floating
	VIO.SW	VIO dc-dc switch	O	P4	P4	VIO.SW	O		Floating
	VIO.GND	VIO dc-dc ground	Power GND	N3	N3	VIO.GND	Power GND		GND
Backup battery	VIO.GND	VIO dc-dc ground	Power GND	P3	P3	VIO.GND	Power GND		GND
	BKBAT	Backup battery	Power	H9	H9	BKBAT	Power		GND
Digital VDD	IO.1P8	TPS65920/TPS65930 device I/O input	Power	B7	B7	IO.1P8	Power		N/A
Digital ground	DGND	Digital ground	Power GND	H10	H10	DGND	Power GND		GND
LED driver	LEDGND	LED driver ground	Power GND	F13	F13	LEDGND	Power GND		GND
	GPIO.13	GPIO13	I/O	B10	B10	GPIO.13	I	PD	Floating
	LEDSYNC	LED synchronization input	I						
	LEDA	LED leg A	Open drain	E13	E13	Signal not functional ⁽³⁾			Floating
	VIBRA.P	H-bridge vibrator P	Open drain	G13	G13	Signal not functional ⁽³⁾			Floating
	LEDB	LED leg B							
	VIBRA.M	H-bridge vibrator M							

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type	TPS65920 Ball	TPS65930 Ball	Default Configuration After Reset Released			Features Not Used ⁽¹⁾
						Signal	Type	Internal Pull or Not	
Keypad	KPD.C0	Keypad column 0	Open drain	G4	G4	KPD.C0	OD		Floating
	KPD.C1	Keypad column 1	Open drain	G3	G3	KPD.C1	OD		Floating
	KPD.C2	Keypad column 2	Open drain	E5	E5	KPD.C2	OD		Floating
	KPD.C3	Keypad column 3	Open drain	B2	B2	KPD.C3	OD		Floating
	KPD.C4	Keypad column 4	Open drain	E3	E3	KPD.C4	OD		Floating
	KPD.C5	Keypad column 5	Open drain	D5	D5	KPD.C5	OD		Floating
	KPD.R0	Keypad row 0	I	K7	K7	KPD.R0	I	PU	Floating
	KPD.R1	Keypad row 1	I	H5	H5	KPD.R1	I	PU	Floating
	KPD.R2	Keypad row 2	I	K5	K5	KPD.R2	I	PU	Floating
	KPD.R3	Keypad row 3	I	H6	H6	KPD.R3	I	PU	Floating
	KPD.R4	Keypad row 4	I	K8	K8	KPD.R4	I	PU	Floating
	KPD.R5	Keypad row 5	I	L8	L8	KPD.R5	I	PU	Floating

(1) This column provides the connection when the associated feature is not used or not connected. When there is a pin muxing, not all Functions on the muxed pin are used. But even if a function is not used, the Default Configuration After Reset Released column still applies.

Connection criteria:

- Analog pins:
 - For input: GND
 - For output: Floating (except VPRECH is connected to GND)
 - For I/O if input by default: GND (except for audio features input: capacitor to ground with a 100-nF typical value capacitor)
- Digital pins:
 - For input: GND (except keypad and STP are left floating)
 - For input and pullup: Floating
 - For output: Floating
 - For I/O and pullup: Floating

N/A (not applicable): When the associated feature is mandatory for the good working of TPS65920/TPS65930 device

(2) The signals VPRECH, VBATS, and VCCS must be connected to each other and with the CPRECH capacitor to GND.

(3) Signal not functional indicates that no signal is presented on the pad after a release reset.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 lists the absolute maximum ratings.

Table 3-1. Absolute Maximum Ratings

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Main battery supply voltage ⁽⁴⁾		2.1		4.5	V
Voltage on any input	Supply represents the voltage applied to the power supply pin associated with the input	0.0		1.0*Supply	V
Storage temperature range		–55		125	°C
Ambient temperature range		–40		85	°C
Junction temperature (T _J)	At 1.4 W (Theta JB 11°C/W 2S2P board)			100	°C
Junction temperature (T _J) for parametric compliance		–40		85	°C

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) The product has negligible reliability impact if voltage spikes of 5.2 V occur for a total duration of 10 milliseconds.

3.2 Minimum Voltages and Associated Currents

Table 3-2 lists the VBAT minimum and maximum currents per VBAT ball.

Table 3-2. VBAT Minimum Required Per VBAT Ball and Associated Maximum Current

Category	Pin and Module	Maximum Current Specified (mA)	Output Voltage (V)	VBAT Minimum (V)
VBAT pin name	VDD_VPLLA3R_IN_6POV	340		
Internal module supplied	VPLL1 (LDO)	40	1.0/1.2/1.3/1.8/2.8/3.0	Maximum (2.7, output voltage selected + 250 mV)
	VDD1 core (DCDC)	< 1		2.7
	VDD2 core (DCDC)	< 1		2.7
	SYSPOR (power ref)	< 1		2.7
	PBIAS (power ref)	< 1		2.7
VBAT pin name	VDD_VDAC_IN_6POV	370		
Internal module supplied	VDAC (LDO)	70	1.2/1.3/1.8	Maximum (2.7, output voltage selected + 250 mV)
	VINTANA1 (LDO)	50	1.5	Maximum (2.7, output voltage selected + 250 mV)
	VINTANA2 (LDO)	250	2.5/2.75	Maximum (2.7, output voltage selected + 250 mV)
	VIO core (DCDC)	< 1		2.7
VBAT pin name	VDD_VAUXI2S_IN_6POV	350		
Internal module supplied	VAUX2 (LDO)	100	1.3/1.5/1.6/1.7/1.8/1.9/2.0/2.1/2.2/2.3/2.4/2.5/2.8	Maximum (2.7, output voltage selected + 250 mV)
VBAT pin name	VDD_VMMC1_IN_6POV	220		
Internal module supplied	VMMC1 (LDO)	220	1.85/2.85/3.0/3.15	Maximum (2.7, output voltage selected + 250 mV)
	Power_REGBATT	0.001		2.7
VBAT pin name	VDD_VINT_IN_6POV	131		

Table 3-2. VBAT Minimum Required Per VBAT Ball and Associated Maximum Current (continued)

Internal module supplied	VINTDIG (LDO)	100	1.0/1.2/1.3/1.5	Maximum (2.7, output voltage selected + 250 mV)
	VRRTC (LDO)	30	1.5	Maximum (2.7, output voltage selected + 250 mV)
	VBACKUP (LDO)	1	2.5/3.0/3.1/3.2	Maximum (2.7, output voltage selected + 250 mV)

3.3 Recommended Operating Conditions

Table 3-3 lists the recommended operating maximum ratings.

Table 3-3. Recommended Operating Maximum Ratings

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Main battery supply voltage		2.7	3.6	4.5	V
Backup battery supply voltage		1.8	3.2	3.3	V
Ambient temperature range		–40		85	°C

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

3.4 Digital I/O Electrical Characteristics

Table 3-4 describes the digital I/O electrical characteristics. The following list defines abbreviations used in the table:

- RL: Reference level voltage applied to the I/O cell
- VOL: Low-level output voltage
- VOH: High-level output voltage
- VIL: Low-level input voltage
- VIH: High-level input voltage
- Min: Minimum value
- Max: Maximum value

Table 3-4. Digital I/O Electrical Characteristics

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIH (V)		Max Freq (MHz)	Load (pF) Output Mode	Rise Time (ns)	Fall Time (ns)
	Min	Max	Min	Max	Min	Max	Min	Max				
GPIO.0/CD1	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	33	30	5.2	5.2
JTAG.TDO												
GPIO.0/CD2	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	33	30	5.2	5.2
JTAG.TMS												
GPIO.2	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
TEST1												
GPIO.15	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
TEST2												
GPIO.6	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
PWM0												
TEST3	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
GPIO.7												
VIBRA.SYNC												
PWM1												
TEST4	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL			5.2	5.2
SYSEN												
CLKEN	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	33.3	33.3
CLKREQ	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3		33.3	33.3
INT1	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	33.3	33.3

Table 3-4. Digital I/O Electrical Characteristics (continued)

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIL (V)		Max Freq (MHz)	Load (pF) Output Mode	Rise Time (ns)	Fall Time (ns)
	Min	Max	Min	Max	Min	Max	Min	Max				
NRESPWRON	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
NRESWARM	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
PWRON					0	0.35×1.8V	0.65×1.8V	VBAT	3		33.3	33.3
NSLEEP1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
CLK256FS	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	6.15	30	16.3	16.3
VMODE1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
BOOT0	0							RL	3		33.3	33.3
BOOT1	0							RL	3		33.3	33.3
REGEN	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
MSECURE	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
I2C.SR.SDA	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4	Up to 400		
VMODE2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3.4		29.4	29.4
I2C.SR.SCL	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4		10.0	10.0
I2C.CNTL.SDA	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4	Up to 400		
I2C.CNTL.SCL	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4		10.0	10.0
I2S.CLK	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	6.5	30	33.0	33.0
I2S.SYNC	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	6.5	30	33.0	33.0
I2S.DIN	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3.25	30	33.0	33.0
I2S.DOUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3.25	30	29.0	29.0
32KCLKOUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.032	30	16	16
HFCLKOUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	38.4	30	2.6	2.6
UCLK	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	60	10	1.0	1.0
STP	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO.9												
DIR	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO.10												
NXT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO.11												
DATA0	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
UART4.TXD												
DATA1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
UART4.RXD												
DATA2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
UART4.RTSI												
DATA3	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
UART4.CTSO												
GPIO.12	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA4	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO.14												
DATA5	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO.3												
DATA6	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO.4												
DATA7	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO.5												
TEST.RESET	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
TEST	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	29.0	29.0
JTAG.TDI/ BERDATA	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
JTAG.TCK/ BERDATA	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
GPIO.13	0	0.45	RL–0.45	RL	0	0.35×RL	0.35×RL		3	30	33.3	33.3
LEDSYNC												
KPD.C0	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0

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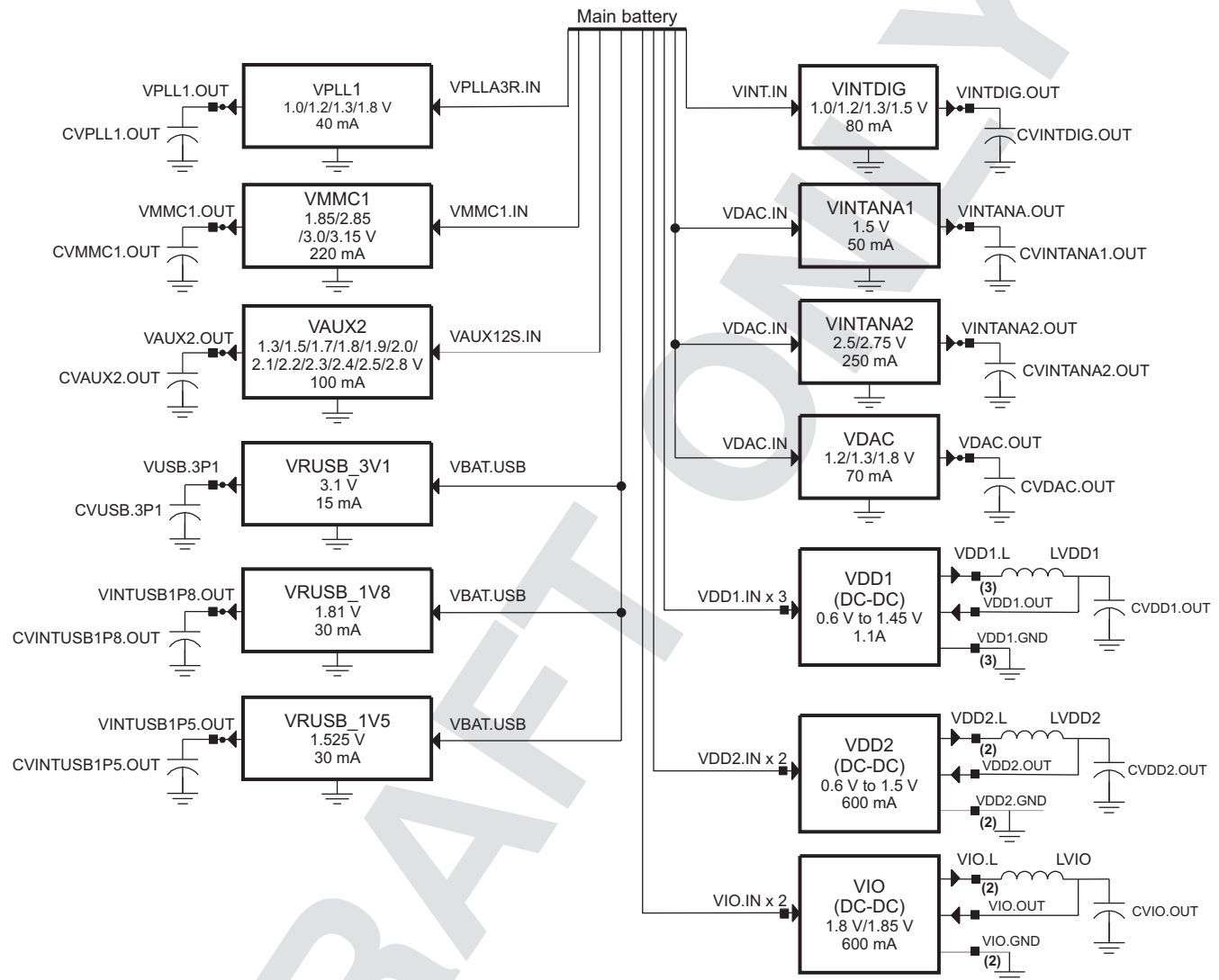
Table 3-4. Digital I/O Electrical Characteristics (continued)

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIL (V)		Max Freq (MHz)	Load (pF) Output Mode	Rise Time (ns)	Fall Time (ns)
	Min	Max	Min	Max	Min	Max	Min	Max				
KPD.C2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C3	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C4	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C5	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.R0	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R3	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R4	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R5	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8

4 Power Module

This section describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled in the TPS65920 and TPS65930 devices.

Figure 4-1 is the power provider block diagram.



037-010

Two internal regulators, VRRTC and VBRTC, are not shown. VRRTC provides power to the RTC, and VBRTC is not used in this configuration.

Figure 4-1. Power Provider Block Diagram

NOTE

For the component values, see [Table 14-1](#).

4.1 Power Providers

Table 4-1 summarizes the power providers.

Table 4-1. Summary of the Power Providers

Name	Usage	Type	Voltage Range (V)	Default Voltage	Maximum Current
VAUX2	External	LDO	1.3, 1.5, 1.7, 1.8, 1.9, 2.0, 2.1, 2.2, 2.3, 2.4, 2.5, 2.8	1.8 V	100 mA
VMMC1	External	LDO	1.85, 2.85, 3.0, 3.15	3.0 V	220 mA
VPLL1	External	LDO	1.0, 1.2, 1.3, 1.8, 2.8, 3.0	1.8 V	40 mA
VDAC	External	LDO	1.2, 1.3, 1.8	1.8 V	70 mA
VIO	External	SMPS	1.8, 1.85	1.8 V	600 mA
VDD1	External	SMPS	0.6 ... 1.45	1.2 V	1100 mA
VDD2	External	SMPS	0.6 ... 1.5	1.2 V	600 mA
VINTANA1	Internal	LDO	1.5	1.5 V	50 mA
VINTANA2	Internal	LDO	2.5, 2.75	2.75 V	150 mA
VINTDIG	Internal	LDO	1.0, 1.2, 1.3, 1.5	1.5 V	100 mA
USBCP	Internal	Charge pump	5	5 V	100 mA
VUSB1V5	Internal	LDO	1.5	1.5 V	30 mA
VUSB1V8	Internal	LDO	1.8	1.8 V	30 mA
VUSB3V1	Internal	LDO	3.1	3.1 V	15 mA
VRRTC	Internal	LDO	1.5	1.5 V	30 mA
VBRTC	Internal	LDO	1.3	1.3 V	100 μ A

4.1.1 VDD1 Dc-dc Regulator

4.1.1.1 VDD1 Dc-dc Regulator Characteristics

The VDD1 dc-dc regulator is a stepdown dc-dc converter with a configurable output voltage. The programming of the output voltage and the characteristics of the dc-dc converter are SmartReflex-compatible. The regulator can be put in sleep mode to reduce its leakage (PFM) or in power-down mode when it is not in use. Table 4-2 describes the regulator characteristics.

Table 4-2. VDD1 Dc-dc Regulator Characteristics

Parameter	Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6		1.45	V
Output voltage step	Covering the 0.6-V to 1.45-V range		12.5		mV
Output accuracy ⁽⁴⁾	0.6 V to < 0.8 V	–6%		6%	
	0.8 V to 1.45 V	–4%		4%	
Switching frequency			3.2		MHz
Conversion efficiency ⁽⁵⁾ , Figure 4-2 in active mode and in sleep mode	I _O = 100 mA, sleep		82%		
	100 mA < I _O < 400 mA		85%		
	400 mA < I _O < 600 mA		80%		
	600 mA < I _O < 1.1 mA		75%		
Output current	Active mode			1.1	A
	Sleep mode			10	mA
Ground current (I _O)	Off at 30°C			3	μA
	Sleep, unloaded		30	50	
	Active, unloaded, not switching			300	
Short-circuit current	V _{IN} = V _{Max}		2.2		A
Load regulation	0 < I _O < I _{Max}			20	mV
Transient load regulation ⁽⁶⁾	I _O = 10 mA to (I _{Max} /2) + 10 mA, Maximum slew rate is I _{Max} /2/100 ns	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV _{PP} ac input, 10-μs rise and fall time			10	mV
Start-up time			0.25	1	ms
Recovery time	From sleep to on with constant load		<10	100	μs
Slew rate (rising or falling) ⁽⁷⁾		4	8	16	mV/μs
Output shunt resistor (pulldown)			150		Ω
External coil	Value	0.7	1	1.3	μH
	Data capture record (DCR)			0.1	Ω
	Saturation current	1.8			A
External capacitor ⁽⁸⁾	Value	8	10	12	μF
	Equivalent series resistance (ESR) at switching frequency	0		20	mΩ

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process)

(5) VBAT = 3.8 V, VDD1 = 1.3 V, Fs = 3.2 MHz, L = 1 μH, L_{DCR} = 100 mΩ, C = 10 μF, ESR = 10 mΩ

(6) Output voltage must discharge the load current completely and settle to its final value within 100 μs.

(7) Load current varies proportionally with the output voltage. The slew rate is for increasing and decreasing voltages, and the maximum load current is 1.1 A.

(8) Under current load condition step:

I_{max}/2 (550 mA) in 100 ns with a ±20% external capacitor accuracy or

I_{max}/3 (367 mA) in 100 ns with a ±50% external capacitor accuracy

See Table 2-2 for how to connect the VDD1/2 dc-dc converter when it is not in use.

Figure 4-2 shows the efficiency of the VDD1 dc-dc regulator in active mode and sleep mode.

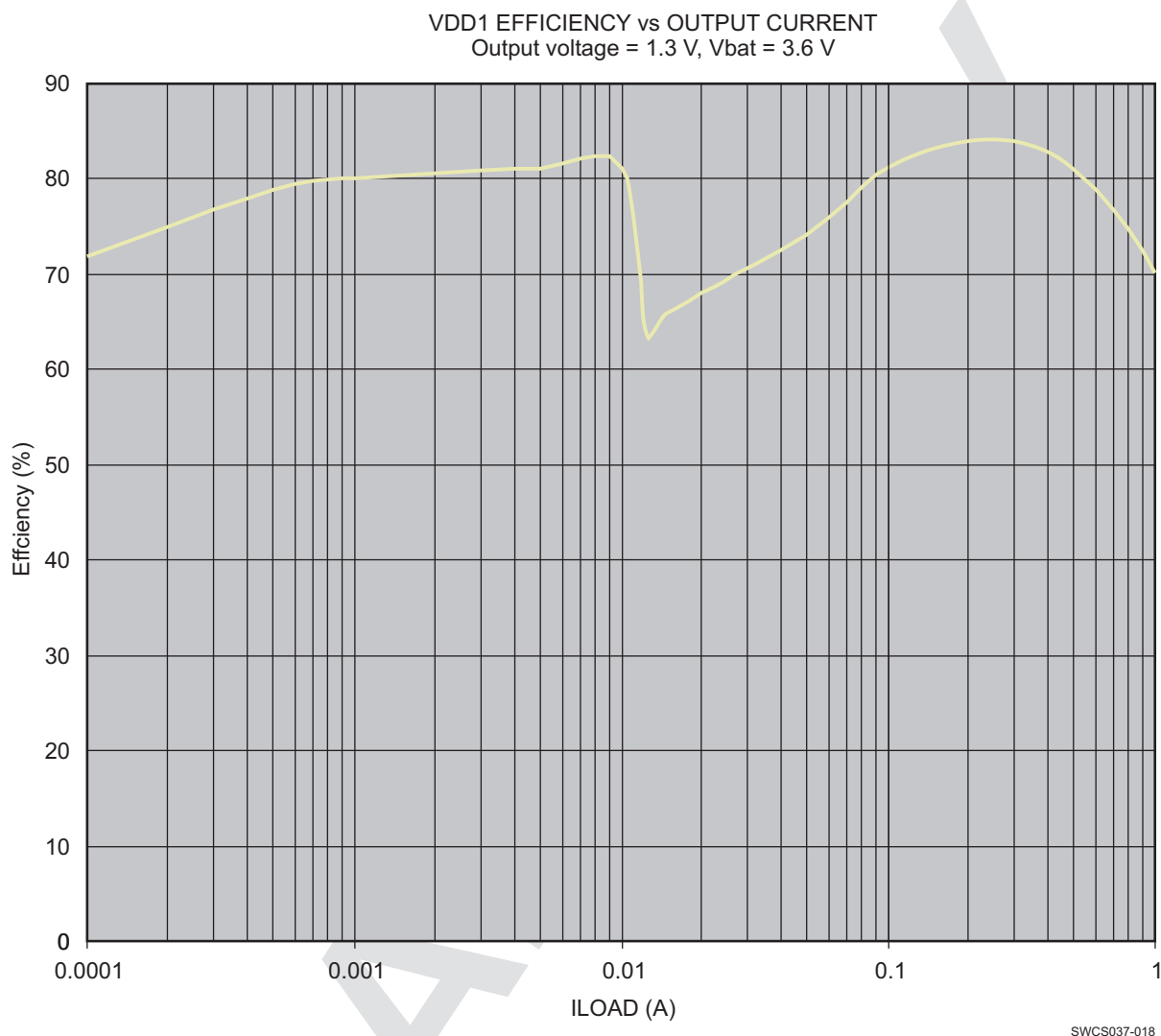


Figure 4-2. VDD1 Dc-dc Regulator Efficiency

4.1.1.2 External Components and Application Schematics

Figure 4-3 is an application schematic with the external components on the VDD1 dc-dc regulator.

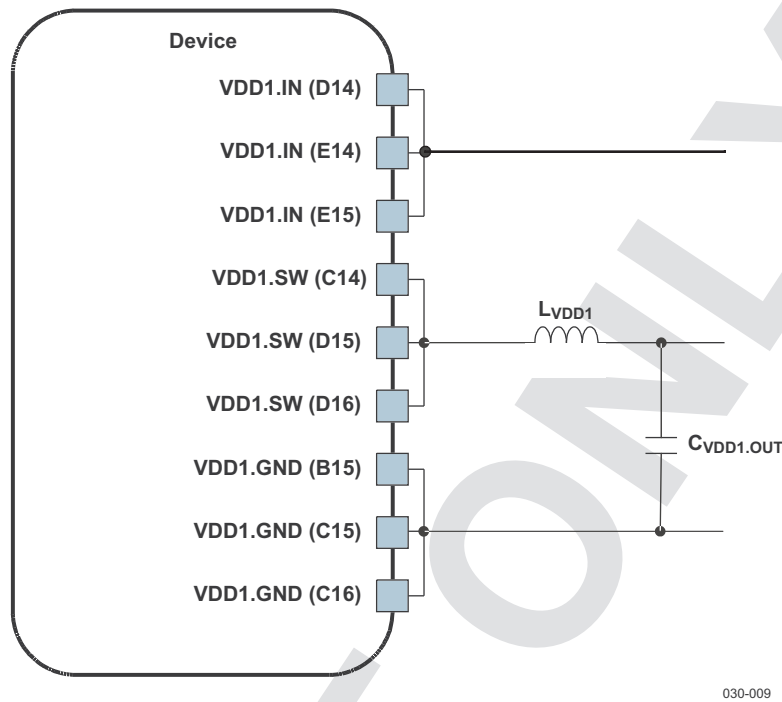


Figure 4-3. VDD1 Dc-dc Application Schematic

NOTE

For the component values, see [Table 14-1](#).

4.1.2 VDD2 Dc-dc Regulator

4.1.2.1 VDD2 Dc-dc Regulator Characteristics

The VDD2 dc-dc regulator is a programmable output stepdown dc-dc converter with an internal field effect transistor (FET). Like the VDD1 regulator, the VDD2 regulator can be placed in sleep or power-down mode and is SmartReflex-compatible. The VDD2 regulator differs from VDD1 in its current load capability. Table 4-3 describes the regulator characteristics.

Table 4-3. VDD2 Dc-dc Regulator Characteristics

Parameter	Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6	1	1.5	V
Output voltage step	Covering the 0.6-V to 1.45-V range, 1.5 V is a single programmable value		12.5		mV
Output accuracy ⁽⁴⁾	0.6 V to < 0.8 V	–6%		6%	
	0.8 V to 1.5 V	–4%		4%	
Switching frequency			3.2		MHz
Conversion efficiency ⁽⁵⁾ , Figure 4-4 in active mode and in sleep mode	I _O = 100 mA, sleep		82%		
	100 mA < I _O < 400 mA		85%		
	400 mA < I _O < 600 mA		80%		
Output current	Active mode			600	mA
	Sleep mode			10	mA
Ground current (I _G)	Off at 30°C			1	μA
	Sleep, unloaded			50	
	Active, unloaded, not switching			300	
Short-circuit current	V _{IN} = V _{Max}		1.2		A
Load regulation	0 < I _O < I _{Max}			20	mV
Transient load regulation ⁽⁶⁾	I _O = 10 mA to (I _{Max} /2) + 10 mA, Maximum slew rate is I _{Max} /2/100 ns	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV _{PP} ac input, 10-μs rise and fall time			10	mV
Output shunt resistor (internal pulldown)			150		Ω
Start-up time			0.25	1	ms
Recovery time	From sleep mode to on mode with constant load		25	100	μs
Slew rate (rising or falling) ⁽⁷⁾		4	8	16	mV/μs
External coil	Value	0.7	1	1.3	μH
	DCR			0.1	Ω
	Saturation current	900			mA
External capacitor ⁽⁸⁾	Value	8	10	12	μF
	ESR at switching frequency	0		20	mΩ

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process)

(5) VBAT = 3.8 V, VDD2 = 1.3 V, F_S = 3.2 MHz, L = 1 μH, L_{DCR} = 100 mΩ, C = 10 μF, ESR = 10 mΩ

(6) Output voltage needs to discharge the load current completely and settle to its final value within 100 μs.

(7) Load current varies proportionally with the output voltage. The slew rate is for both increasing and decreasing voltages and the maximum load current is 600 mA.

(8) Under current load condition step:

I_{max}/2 (300 mA) in 100 ns with a ±20% external capacitor accuracy or

I_{max}/3 (200 mA) in 100 ns with a ±50% external capacitor accuracy

See Table 2-2 for how to connect the VDD1/2 dc-dc converter when it is not in use.

Figure 4-4 shows the efficiency of the VDD2 dc-dc regulator in active mode and sleep mode.

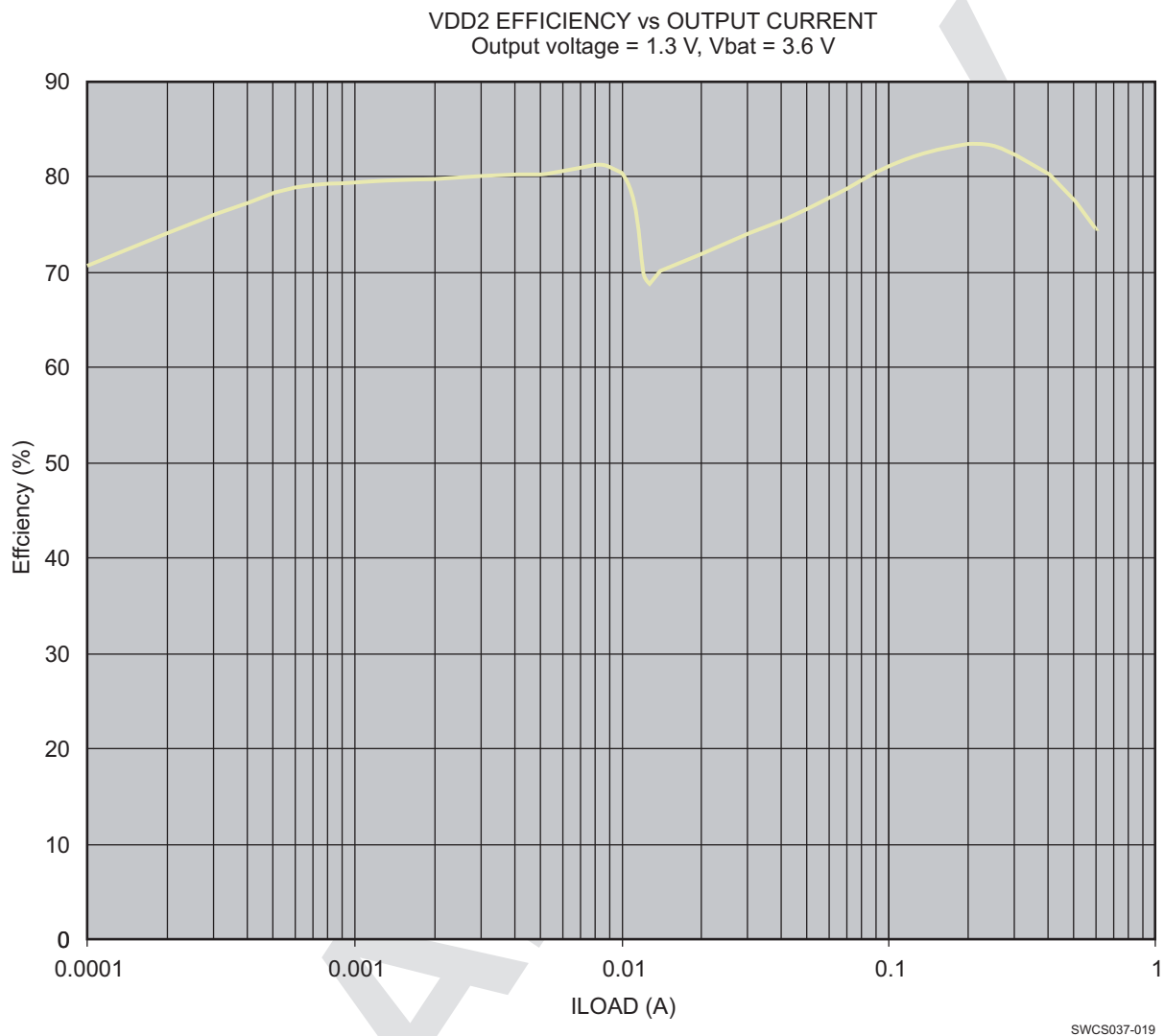


Figure 4-4. VDD2 Dc-dc Regulator Efficiency

4.1.2.2 External Components and Application Schematics

Figure 4-5 is an application schematic with the external components on the VDD2 dc-dc regulator.

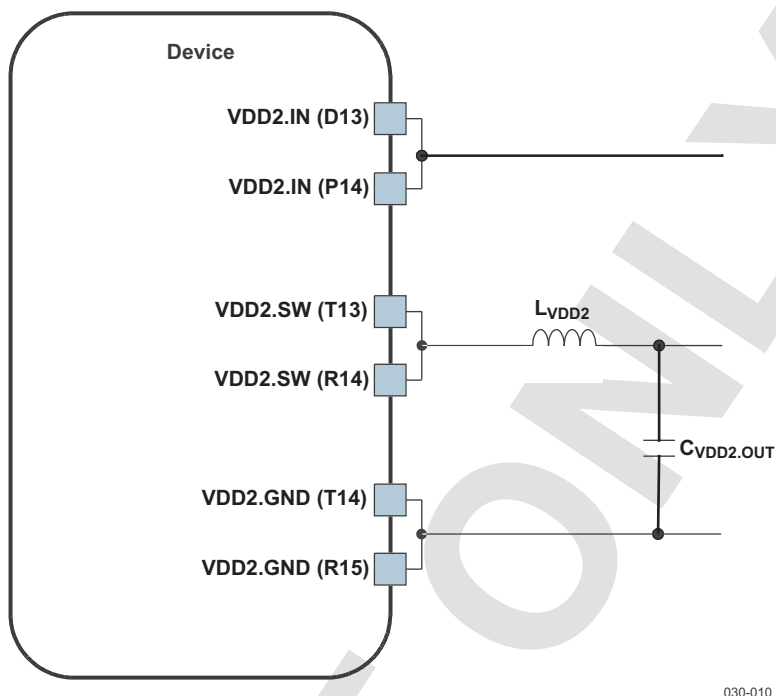


Figure 4-5. VDD2 Dc-dc Application Schematic

NOTE

For the component values, see [Table 14-1](#).

4.1.3 VIO Dc-dc Regulator

4.1.3.1 VIO Dc-dc Regulator Characteristics

The I/O and memory dc-dc regulator is a 600-mA stepdown dc-dc converter (internal FET) with two output voltage settings. It supplies the memories and all I/O ports in the application and is one of the first power providers to switch on in the power-up sequence. This dc-dc regulator can be placed in sleep or power-down mode; however, care must be taken in the sequencing of this power provider, because numerous ESD blocks are connected to this supply. Table 4-4 describes the regulator characteristics.

Table 4-4. VIO Dc-dc Regulator Characteristics

Parameter	Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage ⁽⁴⁾			1.8 1.85		V
Output accuracy ⁽⁵⁾		–4% –3%		4% 3%	
Switching frequency			3.2		MHz
Conversion efficiency ⁽⁶⁾ Figure 4-6 in active mode and in sleep mode	I _O = 10 mA, sleep 100 mA < I _O < 400 mA 400 mA < I _O < 600 mA		85% 85% 80%		
Output current	On mode Sleep mode			600 10	mA
Ground current (I _G)	Off at 30°C Sleep, unloaded Active, unloaded, not switching			1 50 300	μA
Load transient ⁽⁷⁾				50	mV
Line transient	300 mV _{PP} ac, input rise and fall time 10 μs			10	mV
Start-up time			0.25	1	ms
Recovery time	From sleep mode to on mode with constant load		<10	100	μs
External coil	Value DCR Saturation current	0.7	1	1.3 0.1	μH Ω
External capacitor	Value ESR at switching frequency	8 1	10	12 20	μF mΩ

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) This voltage is tuned according to the platform and transient requirements.

(5) ±4% accuracy includes all the variation (line and load regulation, line and load transient, temperature, process)
±3% accuracy is dc accuracy only.

(6) VBAT = 3.8 V, VIO = 1.8 V, Fs = 3.2 MHz, L = 1 μH, L_{DCR} = 100 mΩ, C = 10 μF, ESR = 10 mΩ

(7) Load transient can also be specified as 0 < I_O < I_{OUTmax}/2, Δt = 1 μs, 100 mV but this is not included in ±4% accuracy.

Figure 4-6 shows the efficiency of the VIO dc-dc regulator in active mode and sleep mode.

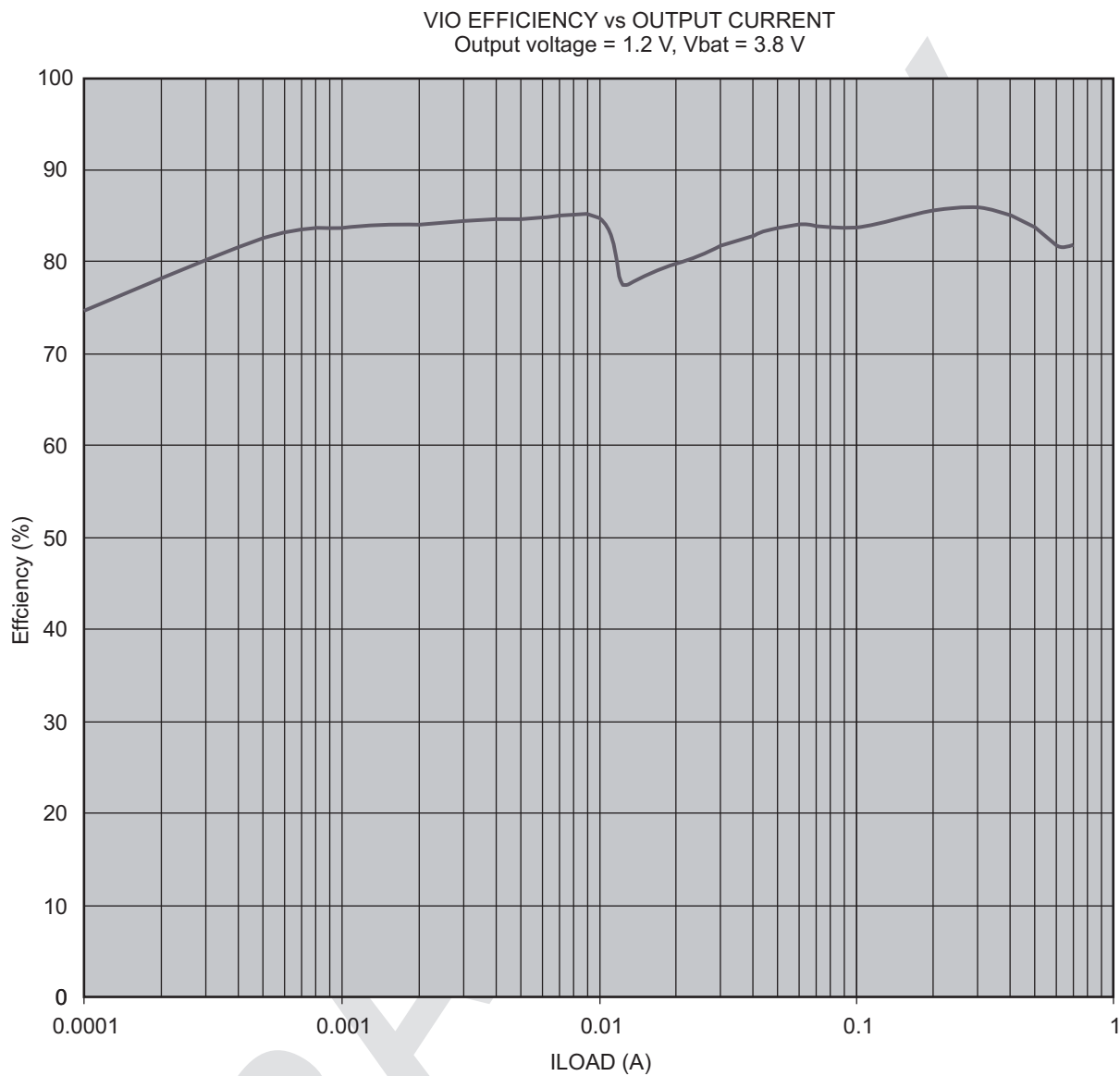


Figure 4-6. VIO Dc-dc Regulator Efficiency

4.1.3.2 External Components and Application Schematics

Figure 4-7 is an application schematic with the external components on the VIO dc-dc regulator.

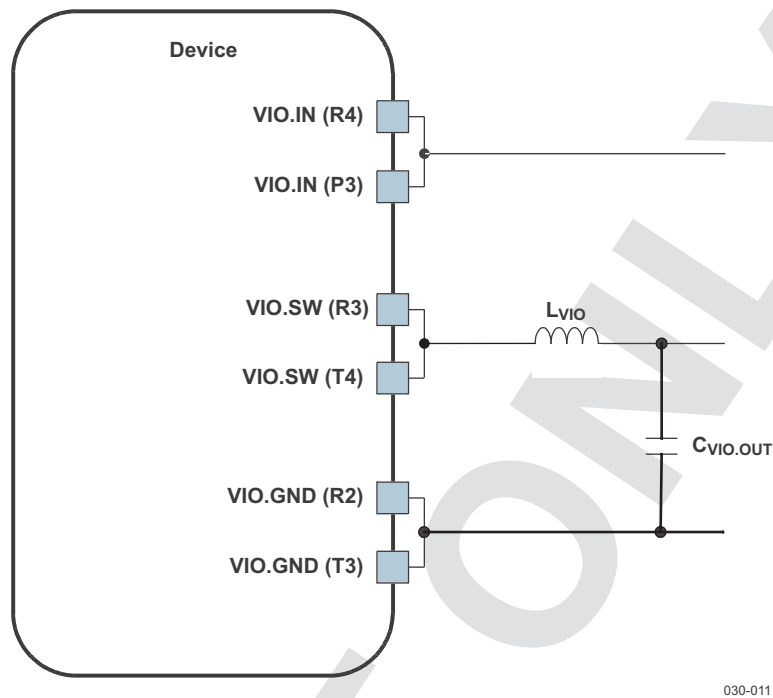


Figure 4-7. VIO Dc-dc Application Schematic

NOTE

For the component values, see [Table 14-1](#).

4.1.4 VDAC LDO Regulator

The VDAC programmable LDO regulator is a high-PSRR, low-noise linear regulator that powers the host processor dual-video DAC. It is controllable with registers through I²C and can be powered down.

Table 4-5 describes the regulator characteristics.

Table 4-5. VDAC LDO Regulator Characteristics

Parameter		Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output Load Conditions						
Filtering capacitor		Connected from VDAC.OUT to analog ground	0.3	1	2.7	μF
Filtering capacitor ESR			20		600	mΩ
Electrical Characteristics						
V _{IN}	Input voltage		2.7	3.6	4.5	V
V _{OUT}	Output voltage	On mode	1.164	1.2	1.236	V
			1.261	1.3	1.339	
			1.746	1.8	1.854	
I _{OUT}	Rated output current	On mode			70	mA
		Low-power mode			1	
Dc load regulation		On mode: 0 < I _O < I _{Max}			20	mV
Dc line regulation		On mode, V _{IN} = V _{INmin} to V _{INmax} at I _{OUT} = I _{OUTmax}			3	mV
Turn-on time		I _{OUT} = 0, C _L = 1 μF (within 10% of V _{OUT})			100	μs
Wake-up time		Full load capability			10	μs
Ripple rejection		f < 20 kHz	65			dB
		20 kHz < f < 100 kHz	45			
		f = 1 MHz	40			
		V _{IN} = V _{OUT} + 1 V, I _O = I _{Max}				
Output noise		100 Hz < f < 5 kHz			400	nV/√Hz
		5 kHz < f < 400 kHz			125	
		400 kHz < f < 10 MHz			50	
Ground current		On mode, I _{OUT} = 0			150	μA
		On mode, I _{OUT} = I _{OUTmax}			350	
		Low-power mode, I _{OUT} = 0			15	
		Low-power mode, I _{OUT} = 1 mA			25	
		Off mode at 55°C			1	
V _{DO}	Dropout voltage	On mode, I _{OUT} = I _{OUTmax}			250	mV
Transient load regulation		I _{Load} : I _{Min} – I _{Max} Slew: 60 mA/μs	–40		40	mV
Transient line regulation		V _{IN} drops 500 mV Slew: 40 mV/μs			10	mV

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

4.1.5 VPLL1 LDO Regulator

The VPLL1 programmable LDO regulator is a high-PSRR, low-noise, linear regulator used for the host processor PLL supply. Table 4-6 describes the regulator characteristics.

Table 4-6. VPLL1 LDO Regulator Characteristics

Parameter		Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output Load Conditions						
Filtering capacitor		Connected from VPLL1.OUT to analog ground	0.3	1	2.7	μF
Filtering capacitor ESR			20		600	mΩ
Electrical Characteristics						
V _{IN}	Input voltage		2.7	3.6	4.5	V
V _{OUT}	Output voltage	On mode and low-power mode	0.97	1.0	1.03	V
			1.164	1.2	1.236	
			1.261	1.3	1.339	
			1.746	1.8	1.854	
			2.716	2.8	2.884	
			2.91	3.0	3.090	
I _{OUT}	Rated output current	On mode			40	mA
		Low-power mode			5	
Dc load regulation		On mode: 0 < I _O < I _{Max}			20	mV
Dc line regulation		On mode, V _{IN} = V _{INmin} to V _{INmax} at I _{OUT} = I _{OUTmax}			3	mV
Turn-on time		I _{OUT} = 0, C _L = 1 μF (within 10% of V _{OUT})			100	μs
Wake-up time		Full load capability			10	μs
	Ripple rejection	f < 10 kHz	50			dB
		10 kHz < f < 100 kHz	40			
		f = 1 MHz	30			
		V _{IN} = V _{OUT} + 1 V, I _O = I _{Max}				
Ground current		On mode, I _{OUT} = 0			70	μA
		On mode, I _{OUT} = I _{OUTmax}			110	
		Low-power mode, I _{OUT} = 0			15	
		Low-power mode, I _{OUT} = 1 mA			16	
		Off mode at 55°C			1	
V _{DO}	Dropout voltage	On mode, I _{OUT} = I _{OUTmax}			250	mV
Transient load regulation		I _{Load} : I _{Min} – I _{Max} Slew: 60 mA/μs	–40		40	mV
Transient line regulation		V _{IN} drops 500 mV Slew: 40 mV/μs			10	mV

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

4.1.6 VMMC1 LDO Regulator

The VMMC1 LDO regulator is a programmable linear voltage converter that powers the multimedia card (MMC) slot. It includes a discharge resistor and overcurrent protection (short-circuit). This LDO regulator can also be turned off automatically when MMC card extraction is detected. The VMMC1 LDO can be powered through an independent supply other than the battery; for example, a charge pump. In this case, the input from the VMMC1 LDO can be higher than the battery voltage. Table 4-7 describes the regulator characteristics.

Table 4-7. VMMC1 LDO Regulator Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output Load Conditions					
Filtering capacitor	Connected from VMMC1.OUT to analog ground	0.3	1	2.7	μF
Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics					
V _{IN} Input voltage		2.7	3.6	5.5	V
V _{OUT} Output voltage	On mode and low-power mode	1.7945 2.7645 2.91 3.0555	1.85 2.85 3.0 3.15	1.9055 2.9355 3.09 3.2445	V
I _{OUT} Rated output current	On mode Low-power mode			220 5	mA
Dc load regulation	On mode: 0 < I _O < I _{Max}			20	mV
Dc line regulation	On mode, V _{IN} = V _{INmin} to V _{INmax} at I _{OUT} = I _{OUTmax}			3	mV
Turn-on time	I _{OUT} = 0, C _L = 1 μF (within 10% of V _{OUT})			100	μs
Wake-up time	Full load capability			10	μs
Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz V _{IN} = V _{OUT} + 1 V, I _O = I _{Max}	50 40 30			dB
Ground current	On mode, I _{OUT} = 0 On mode, I _{OUT} = I _{OUTmax} Low-power mode, I _{OUT} = 0 Low-power mode, I _{OUT} = 5 mA Off mode at 55°C			70 290 17 20 1	μA
V _{DO} Dropout voltage	On mode, I _{OUT} = I _{OUTmax}			250	mV
Transient load regulation	I _{Load} : I _{Min} – I _{Max} Slew: 40 mA/μs	–40		40	mV
Transient line regulation	V _{IN} drops 500 mV Slew: 40 mV/μs			10	mV

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

4.1.7 VAUX2 LDO Regulator

The VAUX2 general-purpose LDO regulator powers the auxiliary devices. Table 4-8 describes the regulator characteristics.

Table 4-8. VAUX2 LDO Regulator Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output Load Conditions					
Filtering capacitor	Connected from VAUX2.OUT to analog ground	0.3	1	2.7	μF
Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics					
V _{IN} Input voltage		2.7	3.6	4.5	V
V _{OUT} Output voltage	On mode and low-power mode	–3%	1.3 1.5 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.8	3%	V
I _{OUT} Rated output current	On mode Low-power mode			100 5	mA
Dc load regulation	On mode: I _{OUT} = I _{OUTmax} to 0			20	mV
Dc line regulation	On mode, V _{IN} = V _{INmin} to V _{INmax} at I _{OUT} = I _{OUTmax}			3	mV
Turn-on time	I _{OUT} = 0, C _L = 1 μF (within 10% of V _{OUT})			100	μs
Wake-up time	Full load capability			10	μs
Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz V _{IN} = V _{OUT} + 1 V, I _O = I _{Max}	50 40 30			dB
Ground current	On mode, I _{OUT} = 0 On mode, I _{OUT} = I _{OUTmax} Low-power mode, I _{OUT} = 0 Low-power mode, I _{OUT} = 5 mA Off mode at 55°C			70 170 17 20 1	μA
V _{DO} Dropout voltage	On mode, I _{OUT} = I _{OUTmax}			250	mV
Transient load regulation	I _{Load} : I _{Min} – I _{Max} Slew: 40 mA/μs	–40		40	mV
Transient line regulation	V _{IN} drops 500 mV Slew: 40 mV/μs			10	mV

- (1) Min = Minimum value
(2) Typ = Typical value
(3) Max = Maximum value

4.1.8 Output Load Conditions

Table 4-9 lists the regulators that power the device, and the output loads associated with them.

Table 4-9. Output Load Conditions

Regulator	Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
VINTDIG LDO	Filtering capacitor	Connected from VINTDIG.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
VINTANA1 LDO	Filtering capacitor	Connected from VINTANA1.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
VINTANA2 LDO	Filtering capacitor	Connected from VINTANA2.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
VRUSB_3V1 LDO	Filtering capacitor	Connected from VUSB.3P1 to GND	0.3	1	2.7	μF
	Filtering capacitor ESR		0	10	600	mΩ
VRUSB_1V8 LDO	Filtering capacitor	Connected from VINTUSB1P8.OUT to GND	0.3	1	2.7	μF
	Filtering capacitor ESR		0	10	600	mΩ
VRUSB_1V5 LDO	Filtering capacitor	Connected from VINTUSB1P5 to GND	0.3	1	2.7	μF
	Filtering capacitor ESR		0	10	600	mΩ

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

4.1.9 Charge Pump

The charge pump generates a 4.8-V (nominal) power supply voltage from the battery to the VBUS pin. The input voltage range is 2.7 to 4.5 V for the battery voltage. The charge pump operating frequency is 1 MHz.

The charge pump tolerates 6 V on VBUS when it is in power-down mode. The charge pump integrates a short-circuit current limitation at 450 mA. Table 4-10 lists the charge pump output load conditions.

Table 4-10. Charge Pump Output Load Conditions

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output Load Conditions					
Filtering capacitor	Connected between VBUS and VSSP	1.41	4.7	6.5	μF
Flying capacitor	Connected between CP and CN	1.32	2.2	3.08	μF
Filtering capacitor ESR				20	mΩ

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

4.1.10 USB LDO Short-Circuit Protection Scheme

The short-circuit current for the LDOs and dc-dcs in the TPS65920 and TPS65930 devices is approximately twice the maximum load current. When the output of the block is shorted to ground, the power dissipation can exceed the 1.2-W requirement if no action is taken. A short-circuit protection scheme is included in the TPS65920 and TPS65930 devices to ensure that if the output of an LDO or dc-dc is short-circuited, the power dissipation does not exceed the 1.2-W level.

The three USB LDOs, VRUSB3V1, VRUSB1V8, and VRUSB1V5, are included in this short-circuit protection scheme, which monitors the LDO output voltage at a frequency of 1 Hz and generates an interrupt (sc_it) when a short-circuit is detected.

The scheme compares the LDO output voltage to a reference voltage and detects a short-circuit if the LDO voltage drops below this reference value (0.5 or 0.75 V programmable). In the case of the VRUSB3V1 and VRUSB1V8 LDOs, the reference is compared with a divided down voltage (1.5 V typical).

If a short-circuit is detected on VRUSB3V1, the power subchip FSM switches this LDO to sleep mode.

If a short-circuit is detected on VRUSB1V8 or VRUSB1V5, the power subchip FSM switches off the relevant LDO.

4.2 Power References

The bandgap voltage reference is filtered (resistance/capacitance [RC] filter) using an external capacitor connected across the VREF output and an analog ground (REFGND). The VREF voltage is scaled, distributed, and buffered in the device. The bandgap is started in fast mode (not filtered), and is set automatically by the power state-machine in slow mode (filtered, less noisy) when required.

Table 4-11 lists the voltage reference characteristics.

Table 4-11. Voltage Reference Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output Load Condition					
Filtering capacitor	Connected from V _{REF} to GNDREF	0.3	1	2.7	μF
Electrical Characteristics					
V _{IN} Input voltage	On mode	2.7	3.6	4.5	V
Internal bandgap reference voltage	On mode, measured through TESTV terminal	1.272	1.285	1.298	V
Reference voltage (V _{REF} terminal)	On mode	0.749	0.75	0.77	V
Retention mode reference	On mode	0.492	0.5	0.508	V
I _{REF} NMOS sink		0.9	1	1.1	μA
Ground current	Bandgap I _{REF} block Preregulator V _{REF} buffer Retention reference buffer			25 20 15 10 10	μA
Output spot noise	100 Hz			1	μV/√Hz
A-weighted noise (rms)			200		nV (rms)
P-weighted noise (rms)			150		nV (rms)
Integrated noise	20 to 100 kHz		2.2		μV
I _{BIAS} trim bit LSB				0.1	μA
Ripple rejection	<1 MHz from VBAT	60			dB
Start-up time				1	ms

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

4.3 Power Consumption

Table 4-12 describes the power consumption depending on the use cases.

NOTE

Typical power consumption is obtained in the nominal operating conditions and with the TPS65920 and TPS65930 devices in stand-alone configuration.

Table 4-12. Power Consumption

Mode	Description	Typical Consumption
Wait on	The phone is apparently off for the user, a main battery is present and well-charged. The RTC registers and registers in the backup domain are maintained. The wake-up capabilities (such as the PWRON button) are available.	VBAT = 3.8 V 64 × 3.8 = 243.2 μW
Active no load	The subsystem is powered by the main battery, all supplies are enabled with full current capability, internal reset is released, and the associated processor is running.	VBAT = 3.8 V 3291 × 3.8 = 12505 μW
Sleep no load	The main battery powers the subsystem, selected supplies are enabled but in low-consumption mode, and the associated processor is in low-power mode.	VBAT = 3.8 V 496 × 3.8 = 1884.4 μW

Table 4-13 lists the regulator states according to the mode in use.

Table 4-13. Regulator State Depending on Use Case

Regulator	Mode			
	Backup	Wait On	Sleep No Load	Active No Load
VAUX2	OFF	OFF	SLEEP	ON
VMMC1	OFF	OFF	OFF	OFF
VPLL1	OFF	OFF	SLEEP	ON
VDAC	OFF	OFF	OFF	OFF
VINTANA1	OFF	OFF	SLEEP	ON
VINTANA2	OFF	OFF	SLEEP	ON
VINTDIG	OFF	OFF	SLEEP	ON
VIO	OFF	OFF	SLEEP	ON
VDD1	OFF	OFF	SLEEP	ON
VDD2	OFF	OFF	SLEEP	ON
VUSB_1V5	OFF	OFF	OFF	OFF
VUSB_1V8	OFF	OFF	OFF	OFF
VUSB_3V1	OFF	OFF	SLEEP	SLEEP

4.4 Power Management

4.4.1 Boot Modes

Only Master C021 mode is supported. Table 4-14 lists the mode corresponding to BOOT0–BOOT1.

Table 4-14. BOOT Mode Description

Mode Name	Mode Description	BOOT0	BOOT1
	Reserved	0	0
	Reserved	0	1
MC021	OMAP3 Boot Mode	1	0
	Reserved	1	1

BOOT0 must be 1 and BOOT1 must be 0.

4.4.2 Process Modes

This parameter defines:

- The boot voltage for the host core
- The boot sequence associated with the process
- The dynamic voltage and frequency scaling (DVFS) protocol associated with the process

4.4.2.1 MC021 Mode

Table 4-15 lists the characteristics of MC021 mode.

Table 4-15. MC021 Mode

Boot core voltage	1.2 V
Power sequence	VIO followed by VPLL1, VDD2, VDD1
DVFS protocol	SmartReflex IF (I ² C HS)

4.4.3 Power-On Sequence

4.4.3.1 Timing Before Sequence_Start

Sequence_Start is a symbolic internal signal to ease the description of the power sequences. It occurs according to the events shown in Figure 4-8.

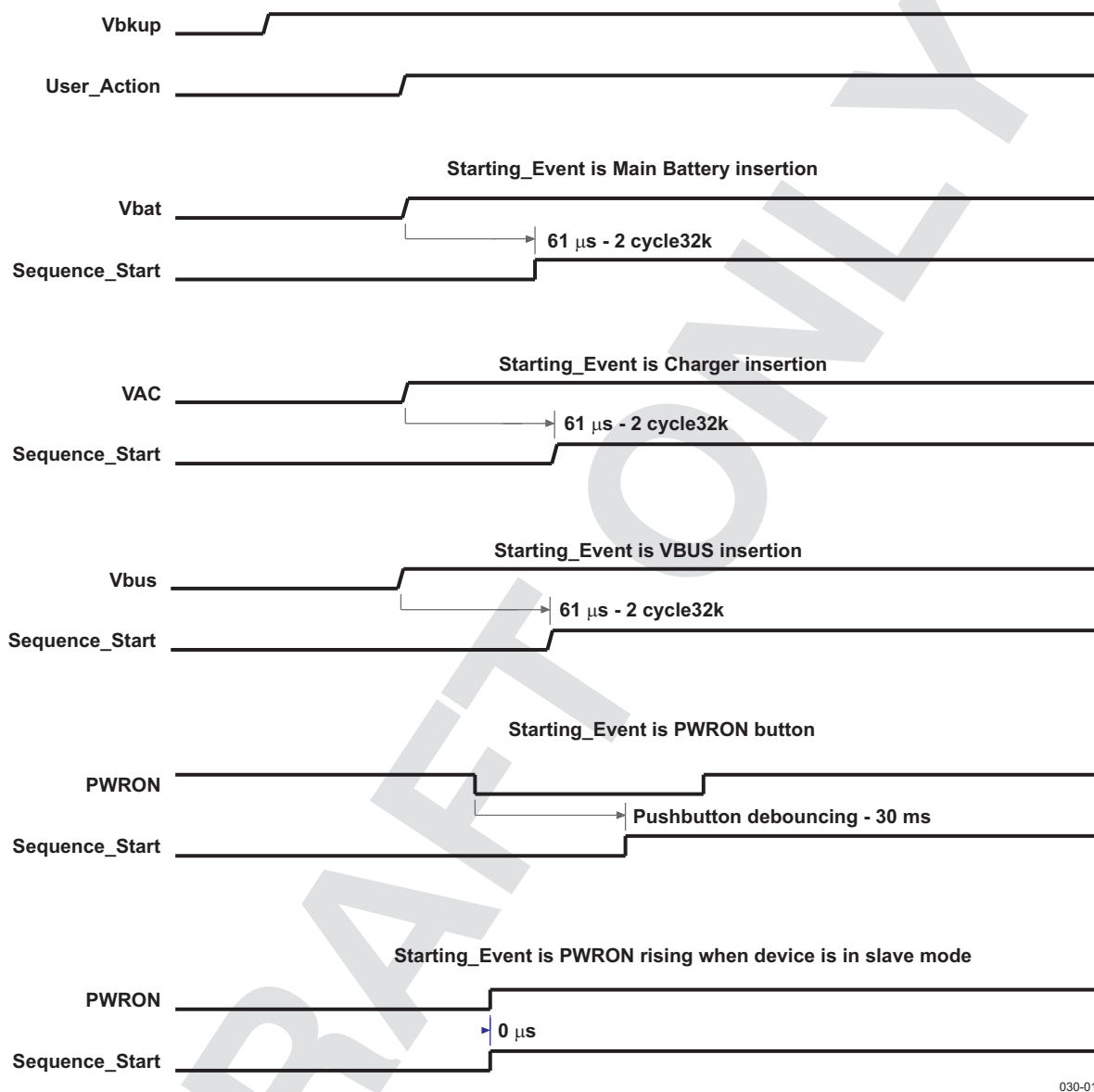
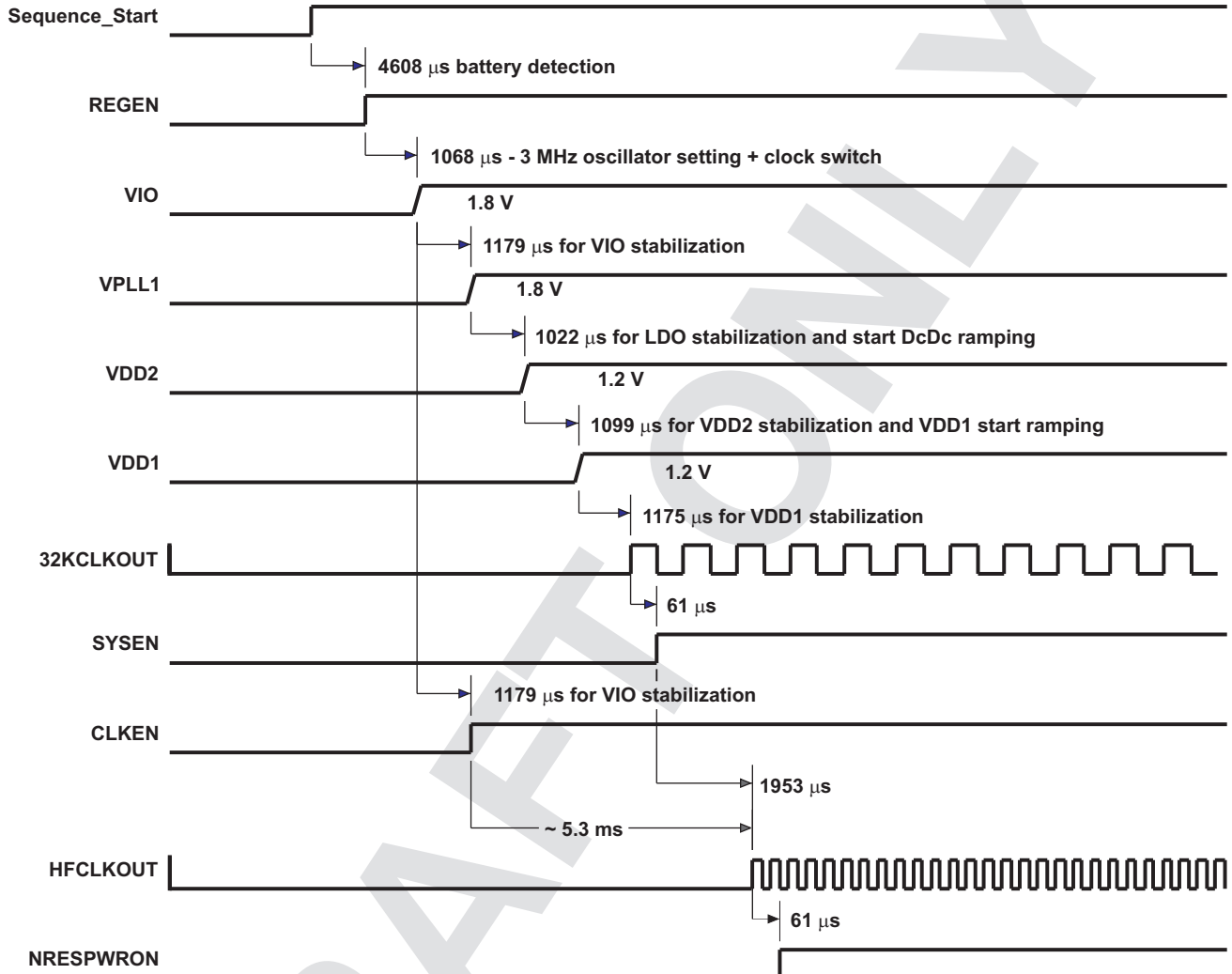


Figure 4-8. Timing Before Sequence_Start

4.4.3.2 Power-On Sequence

Figure 4-9 describes the timing and control that must occur in the OMAP3 mode. Sequence_Start is a symbolic internal signal to ease the description of the power sequences. It occurs according to the events shown in Figure 4-8.



019-072

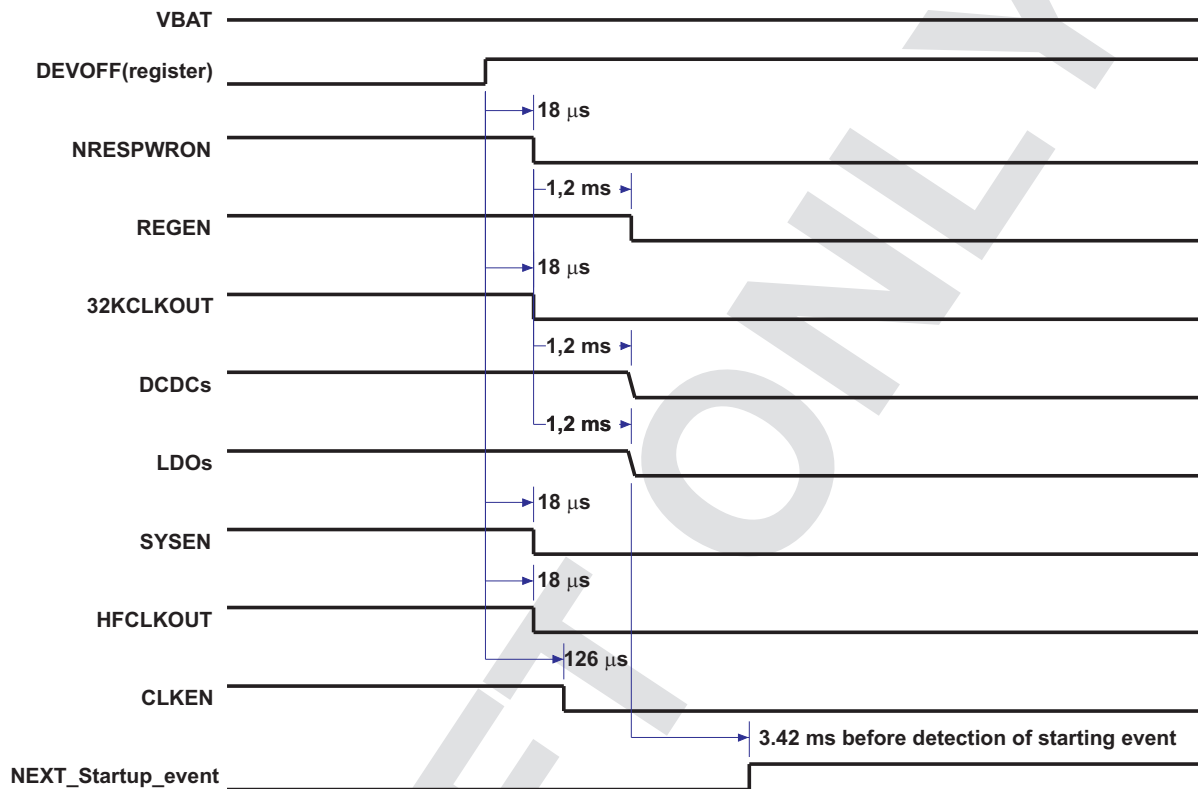
Figure 4-9. Timings–Power On in OMAP3 Mode

4.4.4 Power-Off Sequence

This section describes the signal behavior required to power down the system.

4.4.4.1 Power-Off Sequence

Figure 4-10 shows the timing and control that occur during the power-off sequence in master modes.



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NOTE: All of these timings are typical values with the default setup (depending on the resynchronization between power domains, state machinery priority, etc.).

Figure 4-10. Power-Off Sequence in Master Modes

Because of the internal frequency used by Power STM switching from 3 to 1.5 MHz when the HF clock value is 19.2 MHz, if the HF clock value is not 19.2 MHz (with HFCLK_FREQ bit field values set accordingly in the CFG_BOOT register), the delay between DEVOFF and NRESPWRON/CLK32KOUT/SYSEN/HFCLKOUT is divided by two (approximately 9 µs).

The DEVOFF event is PWRON falling edge in slave mode and DEVOFF internal register write in master mode.

5 Real-Time Clock and Embedded Power Controller

The TPS65930 and TPS65920 devices contain a real-time clock (RTC) module to provide clock and timekeeping functions and an embedded power controller (EPC) to provide battery supervision and control.

5.1 RTC

The RTC provides the following basic functions:

- Time information (seconds/minutes/hours) directly in binary-coded decimal (BCD) code
- Calendar information (day/month/year/day of the week) directly in BCD code
- Interrupt generation periodically (1 second/1 minute/1 hour/1 day) or at a precise time (alarm function)
- 32-kHz oscillator drift compensation and time correction
- Alarm-triggered system wake-up event

5.1.1 Backup Battery

The TPS65030 and TPS65920 devices implement a backup mode in which a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. If the backup battery is rechargeable, the device also provides a backup battery charger so it can be recharged when the main battery supply is present.

The backup domain powers the following:

- Internal 32.768-kHz crystal oscillator
- RTC
- Eight general-purpose (GP) storage registers
- Backup domain low-power regulator (VBRTC)

5.2 EPC

The EPC provides five system states for optimal power use by the system, as listed in [Table 5-1](#).

Table 5-1. System States

System State	Description
NO SUPPLY	The system is not powered by any battery.
BACKUP	The system is powered only with the backup battery and maintains only the VBRTC supply.
WAIT-ON	The system is powered by the main battery and maintains only the VVRTC supply. It can accept switch-on requests.
ACTIVE	The system is powered by the main battery; all supplies can be enabled with full current capability.
SLEEP	The main battery powers the system; selected supplies are enabled, but in low consumption mode.

Three categories of events can trigger state transitions:

- Hardware events: Supply/battery insertion, wake-up requests, USB plug, and RTC alarm
- Software events: Switch-off commands, switch-on commands, and sleep on commands
- Monitoring events: Supply/battery level check, main battery removal, main battery fail, and thermal shutdown

6 Audio/Voice Module (TPS65930 Device Only)

NOTE

This section applies only to the TPS65930 device.

Figure 6-1 is the audio/voice module block diagram.

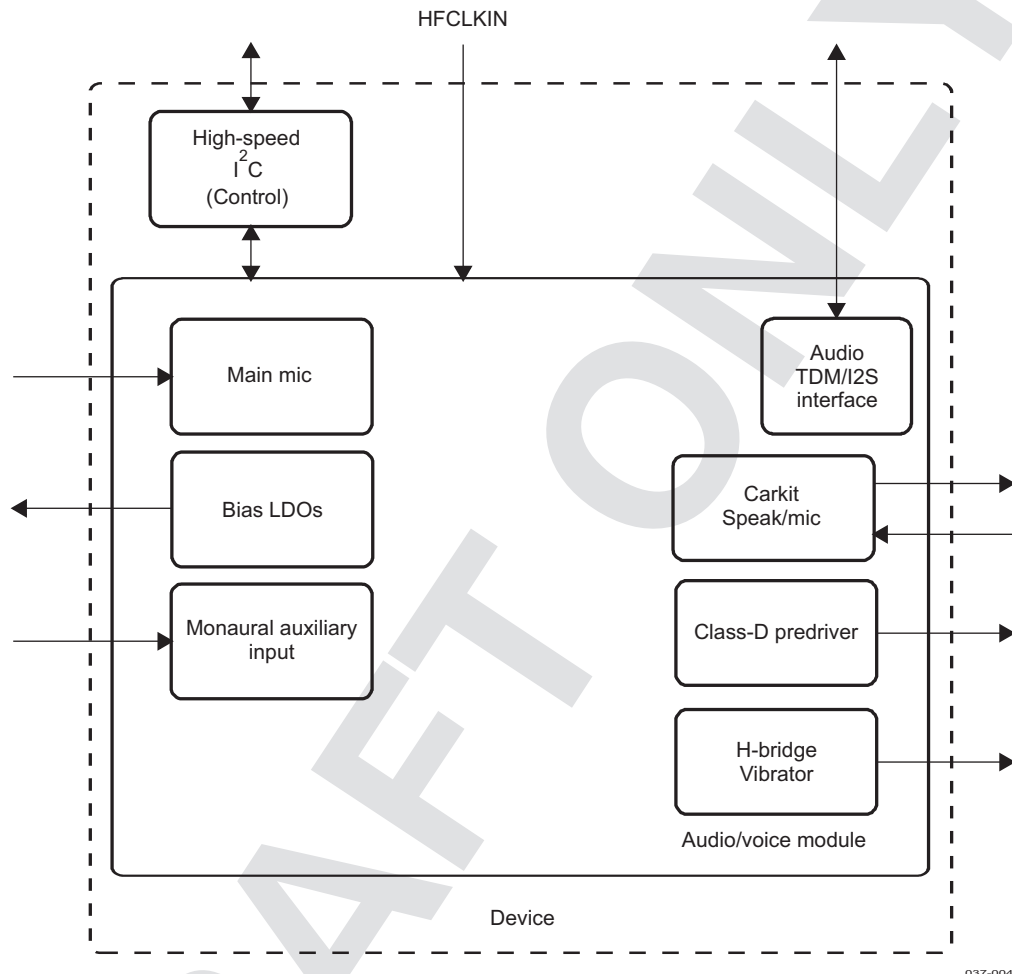


Figure 6-1. Audio/Voice Module Block Diagram

6.1 Audio/Voice Downlink (RX) Module

The audio/voice module includes the following output stages:

- Predriver output signals for external class-D amplifiers (single-ended)
- Vibrator H-bridge

6.1.1 Predriver for External Class-D Amplifier

The external class-D amplifiers provide a stereo signal on terminals PreD.LEFT and PreD.RIGHT to drive the external class-D amplifier. These terminals are available if a stereo, single-ended, ac-coupled headset is used.

6.1.1.1 Predriver Output Characteristics

Table 6-1 lists the predriver output characteristics.

Table 6-1. Predriver Output Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Load impedance		10			kΩ
		50			pF
Gain range ⁽⁴⁾	Audio path	–92		30	dB
	Voice path	–66		30	
Absolute gain error		–1		1	dB
Peak-to-peak output voltage (0 dBfs)	Default gain ⁽⁵⁾		1.5		V _{PP}
Total harmonic distortion	At 0 dBfs		–80	–75	dB
Default gain ⁽⁵⁾	At –6 dBfs		–74	–69	
Load > 10 kΩ // 50 pF	At –20 dBfs		–70	–65	
	At –60 dBfs		–30	–25	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain ⁽⁵⁾ Load = 10 Ω		–90	–85	dB
SNR (A-weighted over 20-kHz bandwidth)	At 0 dBfs	83	88		dB
Default gain ⁽⁵⁾	At –60 dBfs		30		
Output PSRR (for all gains)	20 Hz to 4 kHz		90		dB
	20 Hz to 20 kHz		70		

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Audio digital filter = –62 to 0 dB (1-dB steps) and 0 to 12 dB (6-dB steps)

Voice digital filter = –3 to 12 dB (1-dB steps)

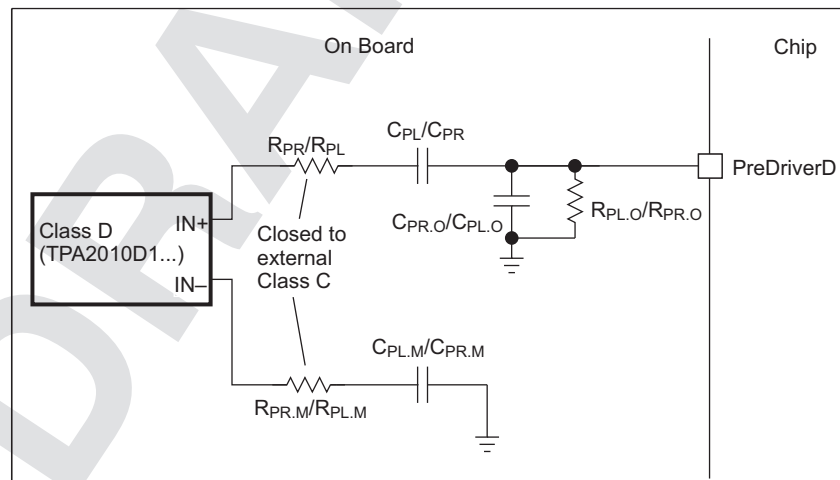
ARXPGA (volume control) = –24 to 12 dB (2-dB steps)

Output driver = –6 dB, 0 dB, 6 dB

(5) The default gain setting assumes the ARXPGA has 0-dB gain setting (volume control) and output driver at 0-dB gain setting.

6.1.1.2 External Components and Application Schematics

Figure 6-2 is a simplified schematic for the external class-D predriver.



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Input resistor (R_{PR} or R_{PL}) sets the gain of the external class D. For TPS2010D1, the gain is defined according to the following equation:

$$\text{Gain (V/V)} = 2 \cdot 150 \cdot 10^3 / (R_{PR} \text{ or } R_{PL})$$

$$R_{PR} \text{ or } R_{PL} > 15 \text{ k}\Omega$$

Figure 6-2. Predriver for External Class D

NOTE

For other component values, see [Table 14-1](#).

6.1.2 Vibrator H-Bridge

A digital signal from the pulse width modulated generator is fed to the vibrator H-bridge driver. The vibrator H-bridge is a differential driver that drives vibrator motors. The differential output allows dual rotation directions.

6.1.2.1 Vibrator H-Bridge Output Characteristics

[Table 6-2](#) lists the vibrator H-bridge output characteristics.

Table 6-2. Vibrator H-Bridge Output Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
VBAT voltage		2.8	3.6	4.8	V
Differential output swing (16-Ω load)	VBAT = 2.8 V	3.6			V _{PP}
	VBAT = 3.5 V	4.3			
Output resistance				4	Ω
Load capacitance				100	pF
Load resistance		8	16	60	Ω
Load inductance			30	300	μH
Total harmonic distortion				10%	
Operating frequency		20		10k	Hz

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

6.1.2.2 External Components and Application Schematics

[Figure 6-3](#) is a simplified vibrator H-bridge schematic.

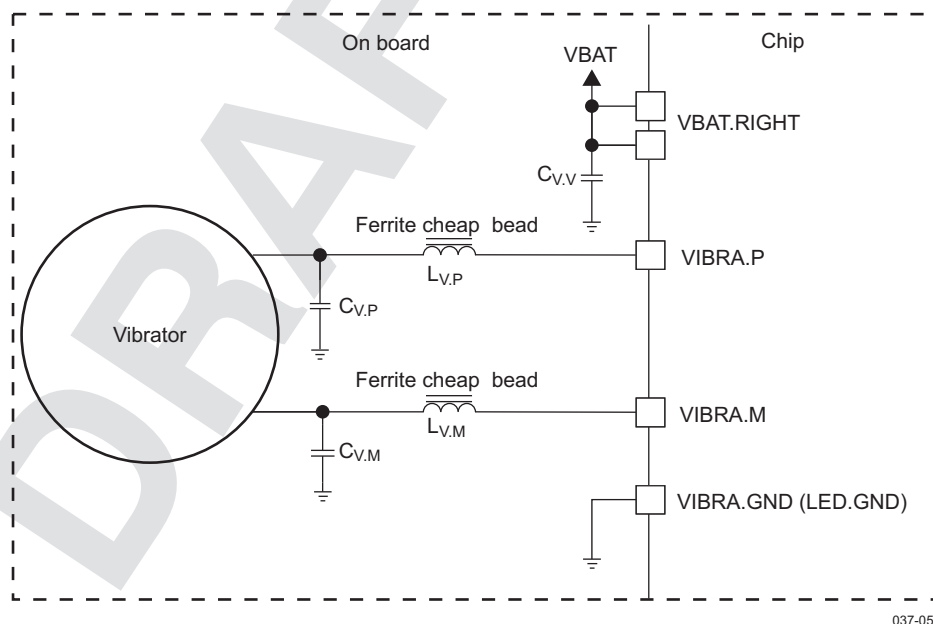


Figure 6-3. Vibrator H-Bridge

NOTE

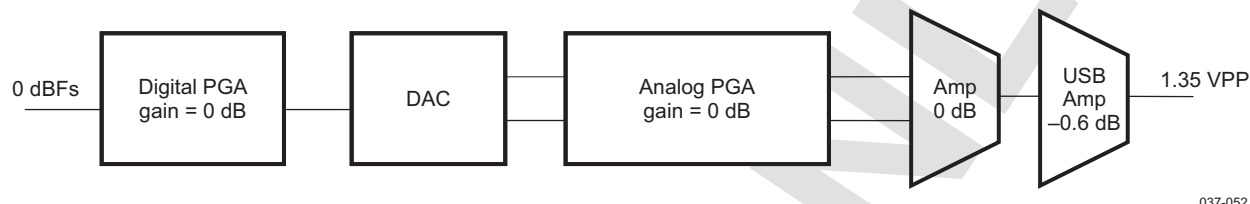
For other component values, see [Table 14-1](#).

Example of ferrite: BLM 18BD221SN1.

6.1.3 Carkit Output

The USB-CEA carkit uses the DP/DM pad to output audio signals (see the *CEA-936–Mini-USB Analog Carkit* specification).

[Figure 6-4](#) shows the carkit output downlink full path characteristics for audio and USB.



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Figure 6-4. Carkit Output Downlink Path Characteristics

[Table 6-3](#) lists the USB-CEA carkit audio downlink electrical characteristics.

Table 6-3. USB-CEA Carkit Audio Downlink Electrical Characteristics

Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output load	USB-CEA (DP/DM)	20			kΩ
Gain range ⁽⁴⁾	Audio path	–92		30	dB
	Voice path	–66		30	
Absolute gain error	At 1 kHz	–1		1	dB
Peak-to-peak differential output voltage (0 dBFS)	Gain = 0 dB		1.5		V _{PP}
Total harmonic distortion	At 0 dBFS		–80	–75	dB
	At –6 dBFS		–74	–69	
	At –20 dBFS		–70	–65	
	At –60 dBFS		–30	–25	
THD+N (20 Hz to 20 kHz, A-weighted)	At 0 dBFS		60		dB
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain ⁽⁵⁾		–90	–85	dB
Output PSRR	20 Hz to 20 kHz		60		dB
Supply voltage (Vintana1)			1.5		V
Common mode output voltage for USB-CEA		1.3	1.35	1.4	V
Isolation between D+/D– during audio mode (20 Hz to 20 kHz)		60			dB
Crosstalk between right and left channels	USB-CEA stereo		–90		dB
Crosstalk RX/Tx (1 V _{PP} output)	USB-CEA mono/stereo			–60	dB
Signal noise ratio (20 Hz to 20 kHz, A-weighted)	At 0 dBFS		60		dB
Phone speaker amplifier output impedance at 1 kHz	USB-CEA (DP/DM)			200	Ω

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Audio digital filter = –62 to 0 dB (1-dB steps) and 0 to 12 dB (6-dB steps)

Voice digital filter = –36 to 12 dB (1-dB steps)

ARXPGA (volume control) = –24 to 12 dB (2-dB steps)

Output driver (USB-CEA) = –1 dB

(5) The default gain setting assumes the ARXPGA has 0-dB gain setting (volume control) and output driver at 0.6-dB gain setting.

6.1.4 Digital Audio Filter Module

Figure 6-5 shows the digital audio filter downlink full path characteristics for the audio interface.

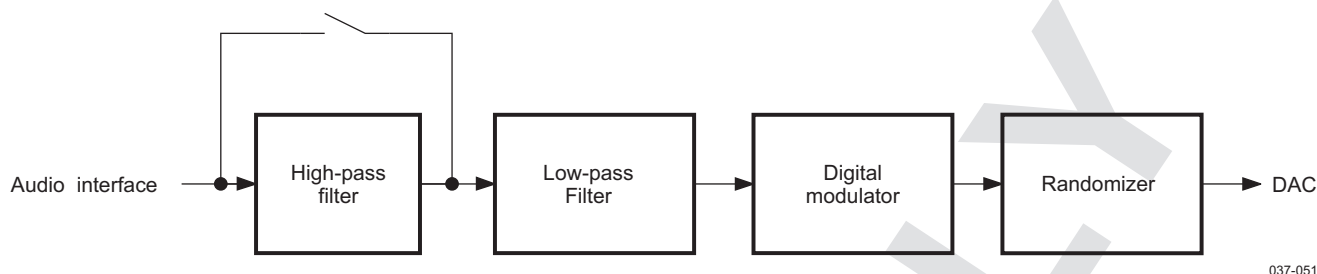


Figure 6-5. Digital Audio Filter Downlink Path Characteristics

The high-pass filter can be bypassed. It is controlled by the MISC_SET_2 ARX_HPF_BYP bit set to address 0x49.

Table 6-4 lists the audio filter frequency responses relative to reference gain at 1 kHz.

Table 6-4. Digital Audio Filter RX Electrical Characteristics

Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Passband			0.42		F _S
Passband ripple	0 to 0.42F _S ⁽⁴⁾	–0.25	0.1	0.25	dB
Stopband			0.6		F _S
Stopband attenuation	F = 0.6F _S ⁽⁴⁾ to 0.8F _S ⁽⁴⁾	60	75		dB
Group delay			15.8/F _S ⁽⁴⁾		μs
Linear phase		–1.4		1.4	°

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) F_S is the sampling frequency (8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz).

6.1.5 Boost Stage

The boost effect adds emphasis to low frequencies. It compensates for a high-pass filter created by the CR (capacitor resistor) filter of the headset (in ac-coupling configuration).

There are four modes. three effects are available, with slightly different frequency responses, and the fourth setting disables the boost effect:

- Boost effect 1
- Boost effect 2
- Boost effect 3
- Flat equalization: The boost effect is in bypass mode.

NOTE

Boost effect modes are defined in Table 6-5.

Table 6-5 and Table 6-6 include the typical values according to the frequency response versus input frequency and F_S frequency.

Table 6-5. Boost Electrical Characteristics Versus F_S Frequency ($F_S \leq 22.05$ kHz)

Frequency (Hz)	$F_S = 8$ kHz			$F_S = 11.025$ kHz			$F_S = 12$ kHz			$F_S = 16$ kHz			$F_S = 22.05$ kHz			Unit
	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	
10	4.51	5.13	5.62	5.10	5.51	5.80	5.22	5.58	5.83	5.54	5.77	5.92	5.76	5.89	5.97	dB
12	4.08	4.83	5.46	4.80	5.32	5.71	4.95	5.41	5.76	5.36	5.66	5.87	5.65	5.83	5.94	
15.2	3.43	4.32	5.18	4.28	4.97	5.54	4.47	5.11	5.61	5.03	5.47	5.79	5.45	5.71	5.90	
18.2	2.91	3.86	4.89	3.82	4.63	5.36	4.04	4.80	5.45	4.71	5.26	5.69	5.24	5.59	5.84	
20.5	2.56	3.53	4.65	3.49	4.37	5.21	3.72	4.56	5.32	4.45	5.09	5.60	5.06	5.49	5.79	
29.4	1.62	2.49	3.78	2.45	3.42	4.57	2.68	3.74	4.73	3.51	4.39	5.24	4.35	5.02	5.59	
39.7	1.05	1.71	2.93	1.67	2.55	3.84	1.88	2.80	4.06	2.66	3.63	4.72	3.67	4.45	5.27	
50.4	0.71	1.20	2.26	1.17	1.91	3.17	1.33	2.13	3.41	2.01	2.95	4.19	2.89	3.85	4.88	
60.3	0.51	0.92	1.79	0.89	1.49	2.65	1.00	1.68	2.89	1.57	2.43	3.72	2.39	3.35	4.52	
76.7	0.32	0.61	1.26	0.59	1.05	1.99	0.69	1.18	2.22	1.11	1.79	3.04	1.76	2.66	3.94	
97.5	0.20	0.39	0.87	0.38	0.70	1.43	0.44	0.79	1.62	0.75	1.27	2.36	1.24	2.00	3.28	
131.5	0.12	0.21	0.50	0.20	0.39	0.88	0.25	0.47	1.02	0.42	0.78	1.59	0.75	1.30	2.41	
157	0.08	0.15	0.36	0.15	0.28	0.65	0.17	0.33	0.75	0.31	0.57	1.22	0.55	0.99	1.93	
200	0.05	0.09	0.22	0.09	0.17	0.41	0.11	0.21	0.49	0.19	0.37	0.82	0.36	0.66	1.38	
240	0.03	0.06	0.15	0.06	0.12	0.29	0.07	0.14	0.35	0.14	0.26	0.60	0.25	0.48	1.04	
304	0.02	0.04	0.09	0.04	0.07	0.18	0.04	0.09	0.22	0.08	0.16	0.38	0.16	0.30	0.70	
463	0.00	0.01	0.03	0.01	0.03	0.07	0.02	0.04	0.09	0.03	0.07	0.17	0.07	0.13	0.32	
704	0.00	0.00	0.01	0.00	0.01	0.03	0.01	0.01	0.03	0.01	0.03	0.07	0.03	0.06	0.14	
1008	0.00	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.01	0.00	0.01	0.03	0.01	0.02	0.06	
1444	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.02	
2070	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	
3770	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	

Table 6-6. Boost Electrical Characteristics Versus F_S Frequency ($F_S \geq 24$ kHz)

Frequency (Hz)	$F_S = 24$ kHz			$F_S = 32$ kHz			$F_S = 44.1$ kHz			$F_S = 48$ kHz			$F_S = 96$ kHz			Unit
	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	
10	5.79	5.90	5.97	5.89	5.89	5.99	5.95	5.98	6.04	5.96	5.99	6.01	5.71	5.83	5.90	dB
12	5.70	5.85	5.95	5.84	5.84	5.98	5.92	5.97	6.03	5.94	5.98	6.00	5.54	5.68	5.81	
15.2	5.53	5.76	5.91	5.73	5.73	5.96	5.87	5.94	6.02	5.89	5.95	5.99	5.40	5.57	5.73	
18.2	5.35	5.65	5.87	5.62	5.62	5.93	5.80	5.90	6.00	5.83	5.93	5.98	5.28	5.48	5.68	
20.5	5.19	5.56	5.83	5.52	5.52	5.91	5.74	5.87	5.99	5.78	5.90	5.97	5.19	5.42	5.64	
29.4	4.55	5.18	5.64	5.10	5.07	5.79	5.51	5.75	5.94	5.57	5.79	5.92	4.87	5.18	5.48	
39.7	3.81	4.62	5.37	4.52	4.52	5.64	5.12	5.53	5.85	5.26	5.59	5.84	4.47	4.91	5.30	
50.4	3.14	4.06	5.02	3.94	3.95	5.43	4.69	5.27	5.72	4.88	5.37	5.73	4.08	4.63	5.11	
60.3	2.62	3.51	4.69	3.46	3.54	5.21	4.30	5.00	5.59	4.49	5.13	5.62	3.72	4.37	4.95	
76.7	1.97	2.90	4.15	2.76	2.76	4.78	3.68	4.52	5.34	3.91	4.70	5.40	3.18	3.92	4.67	
97.5	1.41	2.22	3.51	2.10	2.09	4.27	2.99	3.94	4.99	3.24	4.15	5.07	2.59	3.41	4.33	
131.5	0.88	1.49	2.65	1.40	1.40	3.49	2.15	3.10	4.35	2.38	3.35	4.51	1.86	2.69	3.75	
157	0.65	1.13	2.15	1.04	1.04	2.96	1.70	2.58	3.90	1.90	2.82	4.08	1.47	2.24	3.35	
200	0.41	0.76	1.55	0.70	0.70	2.28	1.19	1.93	3.23	1.35	2.15	3.44	1.03	1.68	2.77	
240	0.30	0.55	1.18	0.50	0.50	1.81	0.89	1.51	2.71	1.02	1.70	2.92	0.77	1.31	2.32	
304	0.18	0.35	0.80	0.33	0.32	1.27	0.58	1.04	2.05	0.68	1.19	2.24	0.51	0.90	1.75	
463	0.08	0.16	0.37	0.14	0.14	0.64	0.27	0.50	1.12	0.31	0.58	1.25	0.23	0.43	0.95	
704	0.03	0.06	0.16	0.06	0.06	0.29	0.12	0.23	0.56	0.14	0.27	0.62	0.10	0.20	0.46	
1008	0.01	0.03	0.07	0.03	0.02	0.14	0.06	0.11	0.30	0.06	0.13	0.31	0.05	0.10	0.23	
1444	0.00	0.01	0.03	0.01	0.01	0.06	0.03	0.05	0.16	0.03	0.06	0.15	0.02	0.05	0.11	
2070	0.00	0.00	0.01	0.00	0.00	0.02	0.01	0.02	0.09	0.01	0.03	0.07	0.01	0.02	0.05	
3770	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.04	0.00	0.00	0.01	0.00	0.00	0.01	

6.2 Audio Uplink (TX) Module

The audio uplink path includes two input amplification stages:

- MIC_MAIN_P, MIC_MAIN_M (differential main handset input)
- AUXR (common terminal: single-ended auxiliary)

NOTE

If two audio inputs are needed, and mic bias is not needed, the AUXR input can be used with MIC_MAIN to provide the two inputs.

6.2.1 Microphone Bias Module

A bias generator provides an external voltage of 2.2 V to bias the analog microphones (MICBIAS1 terminal). The typical output current is 1 mA.

6.2.1.1 Analog Microphone Bias Module Characteristics

Table 6-7 lists the characteristics of the analog microphone bias module.

Table 6-7. Analog Microphone Bias Module Characteristics With Bias Resistor

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Bias voltage			2.2		V
Load current				1	mA
Output noise	P-weighted 20 Hz to 6.6 kHz			1.8	μV_{RMS}
External capacitor		0		200	pF
Internal resistance		50	60	70	k Ω

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

NOTE

If the external capacitor is higher than 200 pF, the analog microphone bias becomes unstable. To stabilize it, add a serial resistor.

Table 6-8 lists the characteristics of the analog microphone bias module with a bias resistor.

Table 6-8. Analog Microphone Bias Module Characteristics With Bias Resistor

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
R_{SB}	$C_{\text{B}} < 200 \text{ pF}$	0			Ω
	$C_{\text{B}} = 100 \text{ pF}$	300			
	$C_{\text{B}} = 1 \text{ }\mu\text{F}$	500			
$R_{\text{B}} + R_{\text{SB}}$			2.2 to 2.7		k Ω

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

Figure 6-6 and Figure 6-7 show the external components and application schematics for the analog microphone.

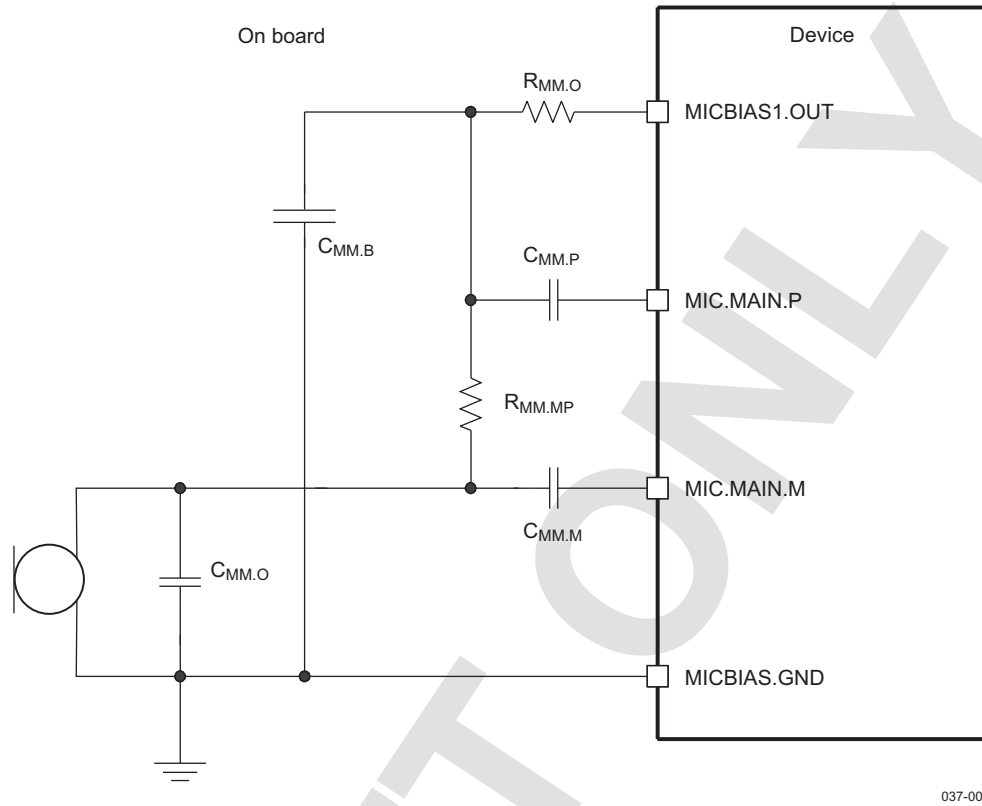
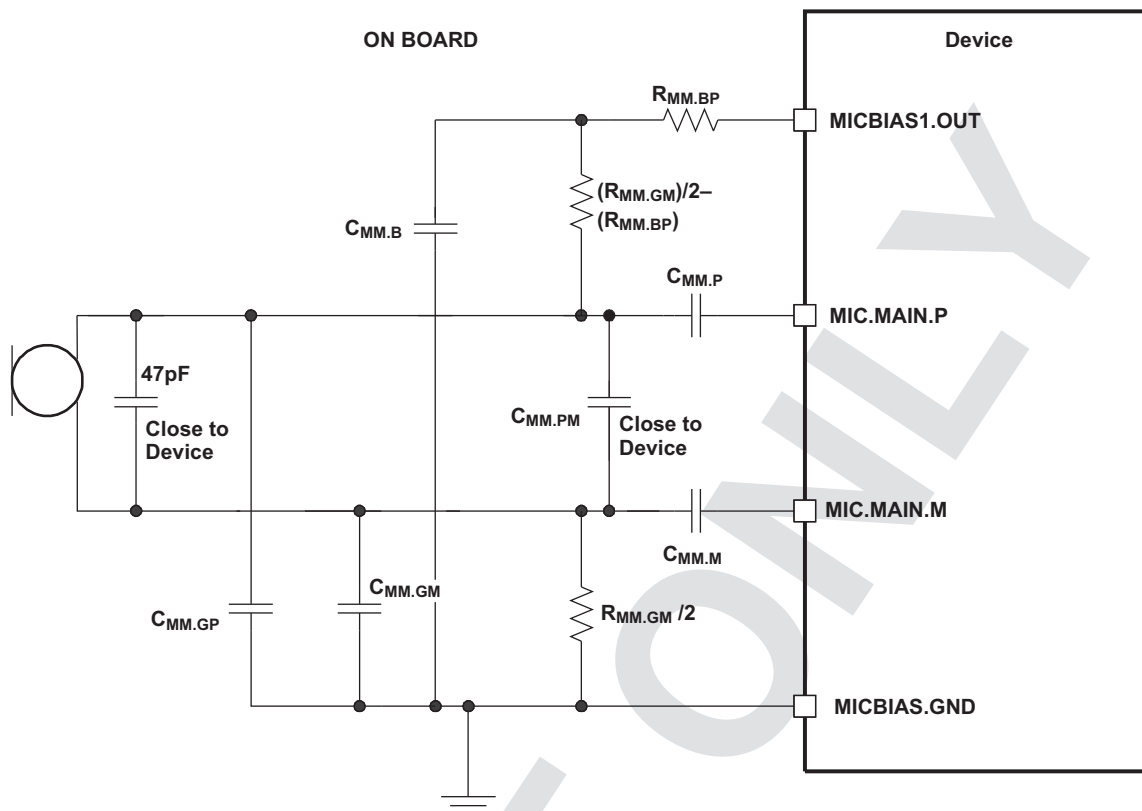


Figure 6-6. Analog Microphone Pseudodifferential

NOTE

For other component values, see [Table 14-1](#).



037-006

Figure 6-7. Analog Microphone Differential

NOTE

For other component values, see [Table 14-1](#).

NOTE

To improve the rejection, ensure that MICBIAS_GND is as clean as possible. This ground must be shared with AGND of the TPS65920 or TPS65930 device and must not share with AVSS4, which is the ground used by RX class AB output stages.

In differential mode, adding a low-pass filter (made by R_{SB} and C_B) is highly recommended if coupling between RX output stages and the microphone is too high (and not enough attenuation by the echo cancellation algorithm). The coupling can come from:

- The internal TPS65920/TPS65930 coupling between MICBIAS.OUT voltage and RX output stages
- Coupling noise between MICBIAS.GND and AVSS4

In pseudodifferential mode, the dynamic resistance of the microphone improves the rejection versus MICBIAS.OUT:

$$PSRR = 20 \cdot \log((R_B + R_{Dyn_mic})/R_B).$$

6.2.1.2 Silicon Microphone Module Characteristics

Based on silicon micro-electrical-mechanical system (MEMS) technology, the new microphone achieves the same acoustic and electrical properties as conventional microphones, but is more rugged and exhibits higher heat resistance. These properties offer designers of a wide range of products greater flexibility and new opportunities to integrate microphones.

The silicon microphone is the integration of mechanical elements and electronics on a common silicon substrate through microfabrication technology.

The complementary metal oxide semiconductor (CMOS) MEMS microphone is more like an analog IC than a classical microphone, or electric condenser microphone (ECM). It is powered as an IC with a direct connection to the power supply. The on-chip isolation between the power input and the rest of the system adds power supply rejection (PSR) to the component. This makes the CMOS MEMS microphone inherently more immune to power supply noise than an ECM and eliminates the need for additional filtering circuitry to keep the power supply line clean.

Table 6-9 lists the characteristics of the silicon microphone module.

Table 6-9. Silicon Microphone Module Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Bias voltage			2.2		V
Load current				1	mA
Output noise	P-weighted 20 Hz to 6.6 kHz			1.8	μV _{RMS}

- (1) Min = Minimum value
(2) Typ = Typical value
(3) Max = Maximum value

Figure 6-8 is a schematic for the silicon microphone.

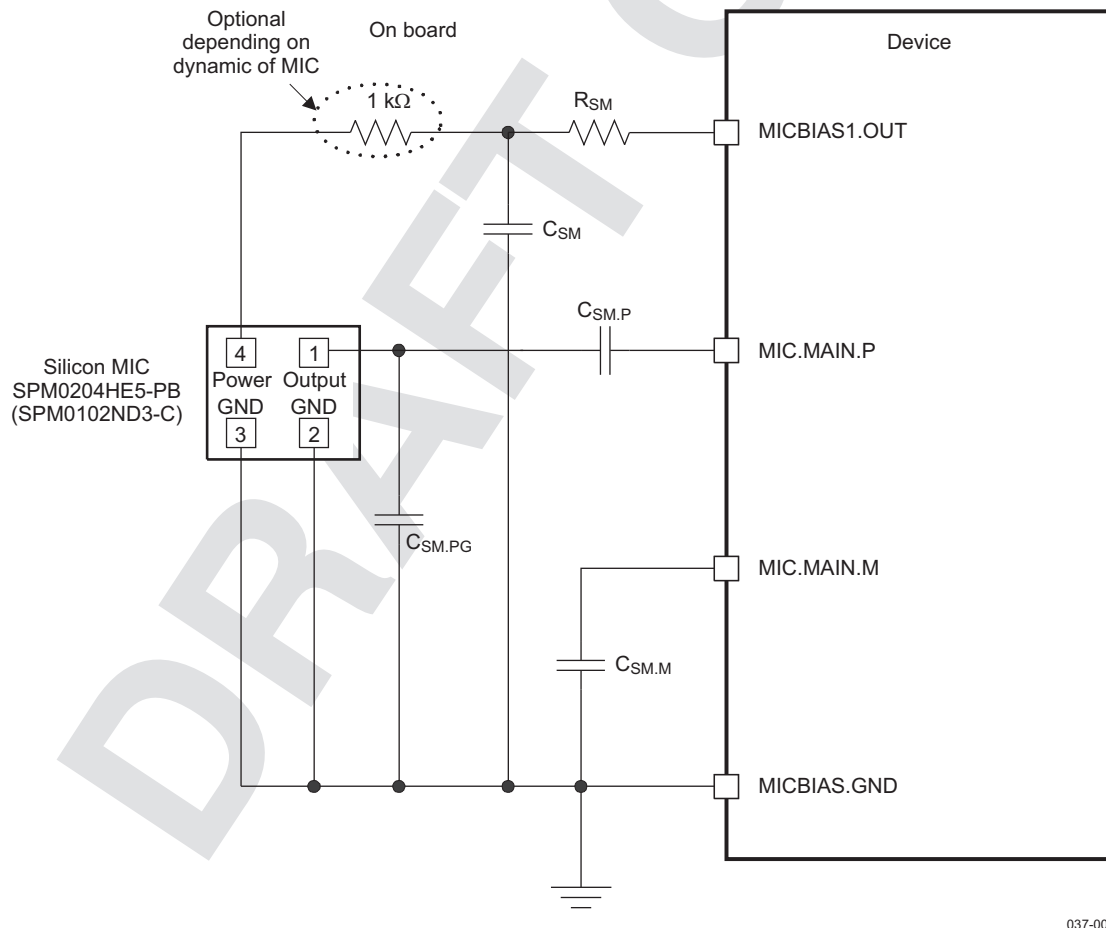


Figure 6-8. Silicon Microphone

NOTE

For other component values, see [Table 14-1](#).

6.2.2 FM Radio/Auxiliary Input

The auxiliary input AUXR/FMR can be used as FM radio input. The amplification stage output is connected to the ADC input. The FM radio input can also be output through an audio output stage.

6.2.2.1 External Components

[Figure 6-9](#) shows the external components on the auxiliary input.

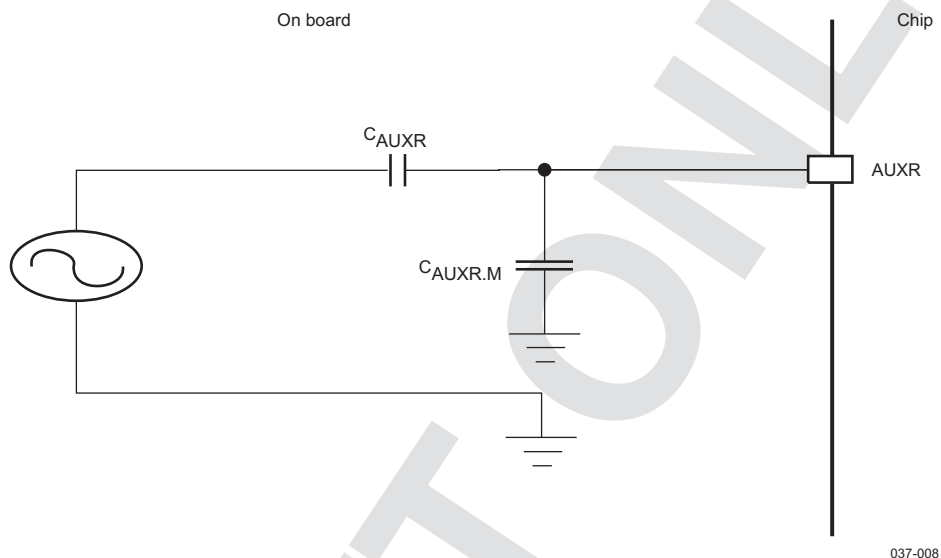


Figure 6-9. Audio Auxiliary Input

NOTE

For other component values, see [Table 14-1](#).

6.2.3 Uplink Characteristics

[Figure 6-10](#) shows the uplink amplifier. [Table 6-10](#) lists the uplink characteristics.

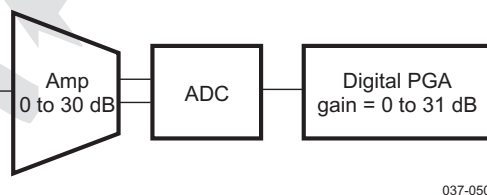


Figure 6-10. Uplink Amplifier

Table 6-10. Uplink Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽²⁾	Unit
Speech delay	Voice path		0.5		ms
Gain range ⁽³⁾		0		61	dB
Absolute gain	0 dBFs at 1.02 kHz	-1		1	dB

(1) Typ = Typical value

(2) Max = Maximum value

(3) Gain range is defined by: Preamplifier = 0 to 30 dB; Filter = 0 to 31 dB (1-dB steps)

Table 6-10. Uplink Characteristics (continued)

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽²⁾	Unit
Peak-to-peak differential input voltage (0 dBFs)	For differential input 0 dB gain setting			1.5	V _{PP}
Peak-to-peak single-ended input voltage (0 dBFs)	For single-ended input 0 dB gain setting			1.5	V _{PP}
Total harmonic distortion (sine wave at 1.02 kHz)	At –1 dBFs		–80	–75	dB
	At –6 dBFs		–74	–69	
	At –10 dBFs		–70	–65	
	At –20 dBFs		–60	–55	
	At –60 dBFs		–20	–15	
Idle channel noise	20 Hz to 20 kHz, A-weighted, gain = 0 dB		–85	–78	dBFs
	16 kHz: < 20 Hz to 7 kHz, gain = 0 dB		–90		
	8 kHz: P-weighted voice, gain = 18 dB		–87		
	16 kHz: < 20 Hz to 7 kHz, gain = 18 dB		–82		
Crosstalk A/D to D/A	Gain = 0 dB		–80		dB
Crosstalk path between two microphones		–70			dB
Intermodulation distortion	2-tone method			–60	dB

6.2.4 Microphone Amplification Stage

The microphone amplification stages perform the single-to-differential conversion for single-ended inputs. Two programmable gains from 0 dB to 30 dB can be set:

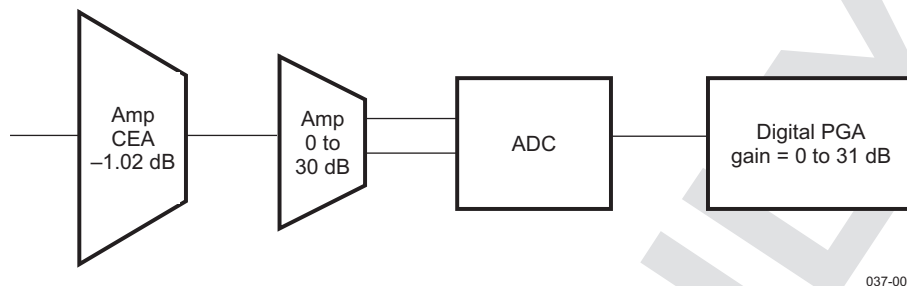
- Automatic level control for main microphone input. The gain step is 1 dB.
- Level control by register for line-in or carkit input. The gain step is 6 dB.

The amplification stage outputs are connected to the ADC input (ADC left and right).

6.2.5 Carkit Input

The USB-CEA carkit uses the DP pad to input the audio signal.

Figure 6-11 shows the uplink carkit full path uplink characteristics for audio and USB.



037-009

Figure 6-11. Carkit Input Uplink Path Characteristics

Table 6-11 lists the USB-CEA carkit audio electrical characteristics.

Table 6-11. USB-CEA Carkit Audio Uplink Electrical Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Gain range ⁽⁴⁾		–1		60	dB
Absolute gain, 0 dBFs at 1.02 kHz ^{(4) (5)}	USB-CEA default gain setting	–1.5		1.5	dB
Speech delay	Voice path		0.5		ms
Input common mode voltage ⁽⁶⁾	USB-CEA	1.3		1.9	V
Phone microphone amplifier input impedance at 1 kHz	USB-CEA	8	120		kΩ
Peak-to-peak single-ended input voltage (0 dBFs)	Default setting			1.414	V _{PP}
Total harmonic distortion (sine wave at 1 kHz), default gain setting	At –1 dBFs		–74	–60	dB
	At –6 dBFs				
	At –10 dBFs				
	At –20 dBFs				
	At –60 dBFs				
THD+N (20 Hz to 20 kHz, A-weighted)	At 0 dBFs		60		dB
Signal noise ratio (20 Hz to 20 kHz, A-weighted)	At 0 dBFs		60		dB
Idle channel noise (20 Hz to 20 kHz, A-weighted), default gain setting	USB-CEA		–77		dBFs
Output PSRR (20 Hz to 20 kHz, A-weighted)	USB-CEA		50		dB

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Gain range is defined by: CEA amplifier = 0.56 dB to –1.02 dB; Preamplifier = 0 to 30 dB; Filter = 0 to 31 dB (1-dB steps).

(5) The CEA default gain setting assumes 0 dB on the preamplifier, 1 dB on digital filter, and CEA amplifier at –1.02 dB.

(6) Full-scale input voltage is 1 V minimum.

6.2.6 Digital Audio Filter Module

Figure 6-12 shows the digital audio filter uplink full path characteristics for the audio interface.

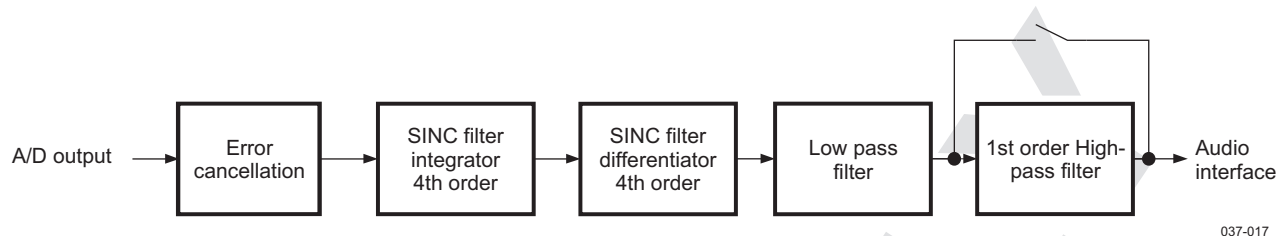


Figure 6-12. Digital Audio Filter Uplink Path Characteristics

The high-pass filter can be bypassed. It is controlled by the MISC_SET_2 ATX_HPF_BYP bit set to address 0x49.

Table 6-12 lists the audio filter frequency responses relative to reference gain at 1 kHz.

Table 6-12. Digital Audio Filter TX Electrical Characteristics

Parameter	Test Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Passband		0.0005		0.42	F _S
Passband gain	In region 0.0005*F _S to 0.42*F _S ⁽⁴⁾	–0.25		0.25	dB
Stopband			0.6		F _S
Stopband attenuation	In region 0.6*F _S to 1*F _S ⁽⁴⁾		60		dB
Group delay			15.8/F _S		μs

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) F_S is the sampling frequency (8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz).

7 USB Transceiver

7.1 USB Transceiver

The TPS65920/TPS65930 device includes a USB OTG transceiver with the CEA carkit interface that supports USB 480 Mbps HS, 12 Mbps full-speed (FS), and USB 1.5 Mbps low-speed (LS) through a 4-pin ULPI.

The carkit block ensures the interface between the phone and a carkit device. The TPS65920/TPS65930 USB supports the CEA carkit standard.

Figure 7-1 is a block diagram of the USB 2.0 physical layer (PHY).

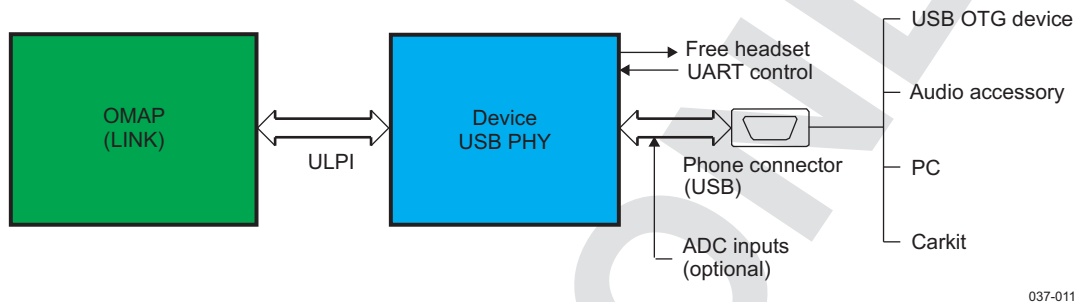


Figure 7-1. USB 2.0 PHY Block Diagram

7.1.1 Features

The device has a USB OTG carkit transceiver that allows system implementation that complies with the following specifications:

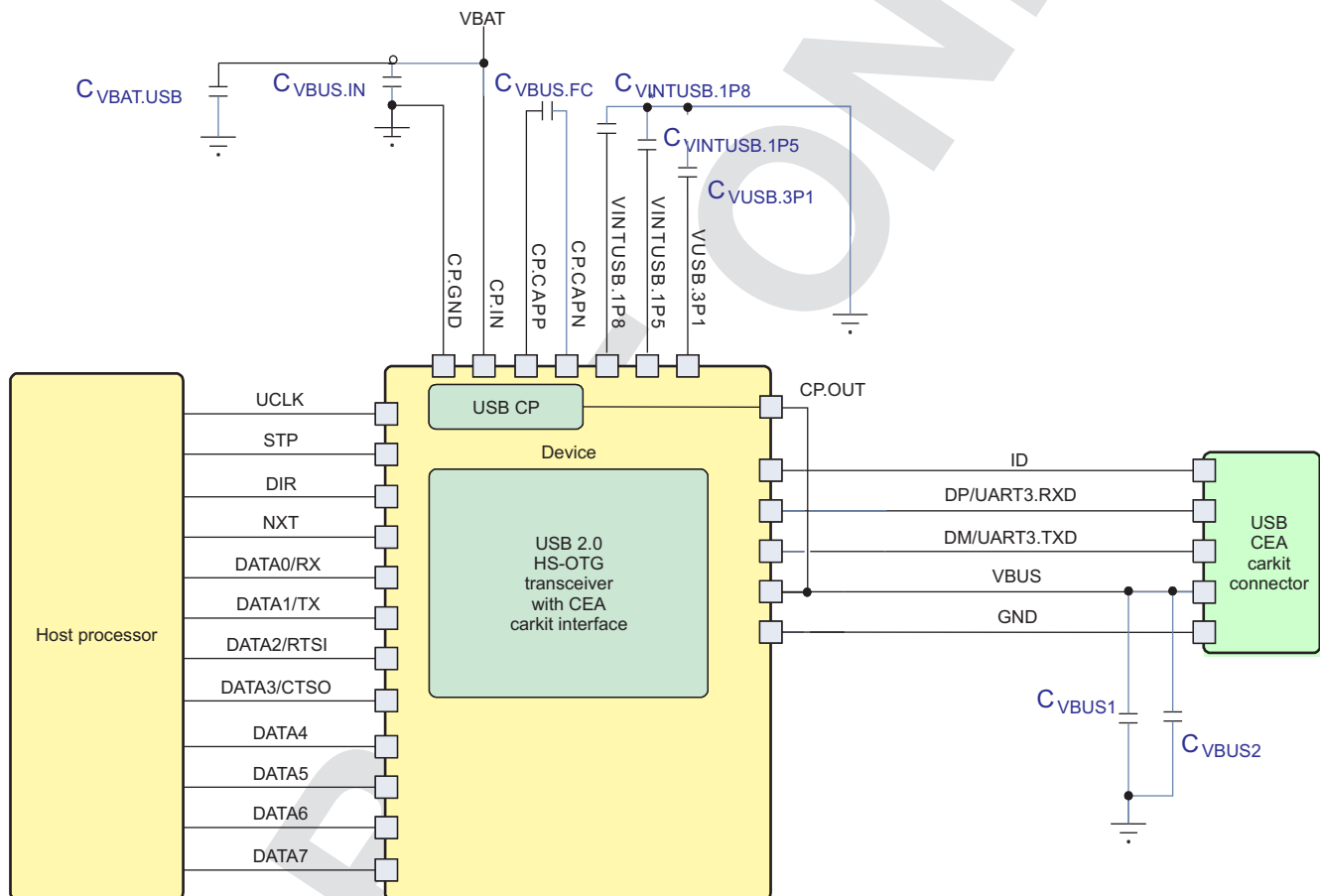
- *Universal Serial Bus 2.0 Specification*
- *On-The-Go Supplement to the USB 2.0 Specification*
- *CEA-2011: OTG Transceiver Interface Specification*
- *CEA-936A: Mini-USB Analog Carkit Specification*
- *UTMI+ Low Pin Interface Specification*

The features of the individual specifications are:

- *Universal Serial Bus 2.0 Specification* (hereafter referred to as the USB 2.0 specification):
 - 5-V-tolerant data line at HS/FS, FS-only, and LS-only transmission rates
 - 7-V-tolerant video bus (VBUS) line
 - Integrated data line serial termination resistors (factory-trimmed)
 - Integrated data line pullup and pulldown resistors
 - On-chip 480-MHz phase-locked loop (PLL) from the internal system clock (19.2, 26, and 38.4 MHz)
 - Synchronization (SYNC)/end-of-period (EOP) generation and checking
 - Data and clock recovery from the USB stream
 - Bit-stuffing/unstuffing and error detection
 - Resume signaling, wakeup, and suspend detection
 - USB 2.0 test modes
- *On-The-Go Supplement to the USB 2.0 Specification* (hereafter referred to as the OTG supplement to the USB 2.0 specification):
 - 3-pin LS/FS serial mode (DAT_SE0)
 - 4-pin LS/FS serial mode (VP_VM)
- *CEA-936A: Mini-USB Analog Carkit Interface Specification* (hereafter referred to as the CEA-936A specification):

- 5-pin CEA mini-USB analog carkit interface
- UART signaling
- Audio (mono/stereo) signaling
- UART transactions during audio signaling
- Basic and smart 4-wire/5-wire carkit, chargers, and accessories
- ID CEA resistor comparators
- *UTMI+ Low Pin Interface Specification* (hereafter referred to as the ULPI specification):
 - 12-pin ULPI with 8-pin parallel data for USB signaling and register access
 - 60-MHz clock generation
 - Register mapping

Figure 7-2 is the USB system application schematic.



037-012

Figure 7-2. USB System Application Schematic

NOTE

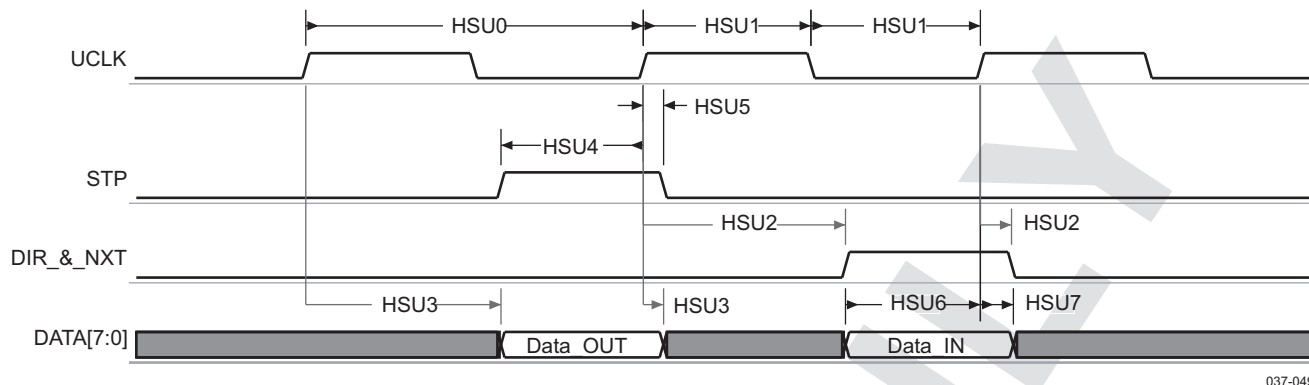
For the component values, see Table 14-1.

7.1.2 HS USB Port Timing

The ULPI interface supports an 8-bit data bus and the internal clock mode. The 4-bit data bus and the external clock mode are not supported.

The HS functional mode supports an operating rate of 480 Mbps.

Table 7-1 and Table 7-2 assume testing over the recommended operating conditions (see Figure 7-3).



037-049

Figure 7-3. HS-USB Interface—Transmit and Receive Modes (ULPI 8-bit)

NOTE

ULPI data [7:0] lines are set to 1 after USB PHY power up, and before the clock signal is stable.

The input timing requirements are given by considering a rising or falling time of 1 ns (see Table 7-1).

Table 7-1. HS-USB Interface Timing Requirements

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
HSU4	$t_{s(STPV-CLKH)}$	Setup time, STP valid before UCLK rising edge	6		ns
HSU5	$t_{h(CLKH-STPIV)}$	Hold time, STP valid after UCLK rising edge	0		ns
HSU6	$t_{s(DATAV-CLKH)}$	Setup time, DATA[0:7] valid before UCLK rising edge	6		ns
HSU7	$t_{h(CLKH-DATV)}$	Hold time, DATA[0:7] valid after UCLK rising edge	0		ns

(1) Min = Minimum value

(2) Max = Maximum value

Table 7-2 lists the HS-USB interface switching requirements.

Table 7-2. HS-USB Interface Switching Requirements⁽¹⁾

Notation	Parameter ⁽¹⁾			Min ⁽²⁾	Typ ⁽³⁾	Max ⁽⁴⁾	Unit
HSU0	$f_{p(CLK)}$	UCLK clock frequency	Steady state	58.42	60	61.67	MHz
HSU1	$t_{W(CLK)}$	UCLK duty cycle	Steady state	48.3%	50%	51.7%	
HSU2	$t_{d(CLKH-DIR)}$	Delay time, UCLK rising edge to DIR transition	Steady state	0		9	ns
	$t_{d(CLKH-NXTV)}$	Delay time, UCLK rising edge to NXT transition	Steady state	0		9	ns
HSU3	$t_{d(CLKH-DATV)}$	Delay time, UCLK rising edge to DATA[0:7] transition	Steady state	0		9	ns

(1) The capacitive load for output data and control load is 10 pF (rising and falling time is 2 ns).

The capacitive load for the CLK port is 6 pF (rising and falling time is 1 ns).

The HS-USB interface has only one state: the steady-state.

(2) Min = Minimum value

(3) Typ = Typical value

(4) Max = Maximum value

7.1.3 USB-CEA Carkit Port Timing

This mode allows the link for communication through the USB PHY to a remote carkit in CEA audio + data during audio (DDA) mode as defined in the CEA-936A specification. In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

UART data are sent and received on the USB D+/D– pads. D+/D– are also used in this mode to carry audio I/O signals.

Table 7-3 assumes testing over the recommended operating conditions (see the CEA-936A specification).

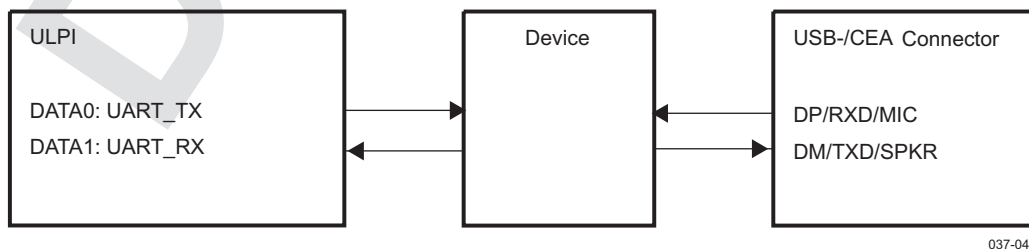
Table 7-3. USB-CEA Carkit Interface Timing Parameters

Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
t _{PH_DP_CON}	Phone D+ connect time	100		ms
t _{CR_DP_CON}	Carkit D+ connect time	150	300	ms
t _{PH_DM_CON}	Phone D– connect time		10	ms
t _{PH_CMD_DLY}	Phone command delay	2		ms
t _{PH_MONO_ACK}	Phone mono acknowledge		10	ms
t _{PH_DISC_DET}	Phone D+ disconnect time	150		ms
t _{CR_DISC_DET}	Carkit D– disconnect detect	50	150	ms
t _{PH_AUD_BIAS}	Phone audio bias	1		ms
t _{CR_AUD_DET}	Carkit audio detect	400	800	μs
t _{CR_UART_DET}	Carkit UART detect (data-during-audio enabled)	700	1200	ns
t _{PH_STLO_DET}	Phone stereo D+ low detect	30	100	ms
t _{PH_PLS_POS}	Phone D– interrupt pulse width	200	600	ns
t _{CR_PLS_NEG}	Carkit D+ interrupt pulse width	200	600	ns
t _{DAT_AUD_POL}	Data-during-audio polarity	20	60	ms
t _{ACC_COL_DET}	Accessory ID collision detect	2	3	ms
t _{ACC_INT_PW}	Accessory ID interrupt pulse width	200	400	μs
t _{ACC_INT_WAIT}	Accessory ID interrupt wait time	10	15	ms
t _{ACC_CMD_WAIT}	Accessory ID command wait time	0		ms
t _{PH_INT_PW}	Phone ID interrupt pulse width	4	8	ms
t _{PH_INT_WAIT}	Phone ID interrupt wait time	4	8	ms
t _{PH_CMD_WAIT}	Phone ID command wait time	0		ms
t _{PH_UART_RPT}	Phone command repeat time	50		ms
t _{CR_UART_RSP}	Carkit UART response		30	ms
t _{CR_INT_RPT}	Carkit interrupt repeat time	50		ms
f _{UART_DFLT}	Default UART signaling rate (typical rate)		9600	bps

(1) Min = Minimum value

(2) Max = Maximum value

Figure 7-4 shows the USB-CEA carkit UART data flow.



037-048

Figure 7-4. USB-CEA Carkit UART Data Flow

[Table 7-4](#) lists the USB-CEA carkit UART timings.

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Table 7-4. USB-CEA Carkit UART Timings

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
CK1	$t_{d(UART_TXH-DM)}$	Delay time, UART_TX rising edge to DM transition	4.0	11	ns
CK2	$t_{d(UART_TXL-DM)}$	Delay time, UART_TX falling edge to DM transition	4.0	11	ns
CK3	$t_{d(DPH-UART_RX)}$	Delay time, DP rising edge to UART_RX transition	At 38.4 MHz	205	ns
			At 19.2 MHz	310	
CK4	$t_{d(DPL-UART_RX)}$	Delay time, DP falling edge to UART_RX transition	At 38.4 MHz	205	ns
			At 19.2 MHz	310	

(1) Min = Minimum value

(2) Max = Maximum value

Figure 7-5 shows the USB-CEA carkit UART timings.

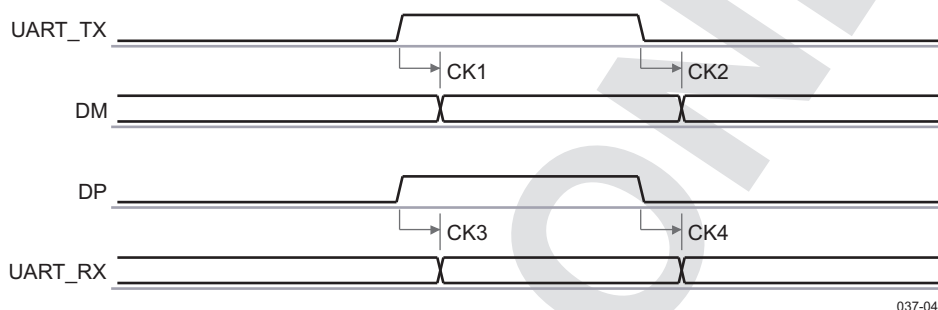


Figure 7-5. USB-CEA Carkit UART Timings

7.1.4 PHY Electrical Characteristics

The PHY is the physical signaling layer of the USB 2.0. It contains the drivers and receivers for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces with the USB controller through the UTMI.

The transmitters and receivers in the PHY are of two main classes:

- FS and LS transceivers (legacy USB1.x transceivers)
- HS transceivers

To bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A DPLL that does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB, and the clock required for the switched capacitor resistance block
- A switched capacitor resistance block that replicates an external resistor on chip

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

The PHY also contains circuitry that protects it from an accidental 5-V short on the DP and DM lines and from 8-kV IEC ESD strikes.

7.1.4.1 HS Differential Receiver

The HS receiver consists of the following blocks:

- A differential input comparator to receive the serial data
- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a nonreturn to zero inverted (NRZI) decoder, bit unstuffing, and serial-to-parallel converter to generate the UTMI DATAOUT

Table 7-5 lists the characteristics of the HS differential receiver.

Table 7-5. HS Differential Receiver

Parameter		Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Input Levels for HS						
HS squelch detection threshold	V _{HSSQ}	(Differential signal amplitude)	100	125	150	mV
HS disconnect detection threshold	V _{HSDSC}	(Differential signal amplitude)	525	600	625	mV
HS data signaling common mode voltage range	V _{HSCM}		–50	200	500	mV
HS differential input sensitivity	V _{DIHS}	(Differential signal amplitude)	–100		100	mV
Input Impedance for HS						
Internal specification for input capacitance	C _{HSLOAD}			11		pF
Internal C _{HSLOAD} DP/DM matching	C _{HSLOADM}			0.2		pF
External Components With the Total Budget Combined (without USB cable load)						
External capacitance on DP or DM					2	pF
External series resistance on DP or DM					1	Ω

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

7.1.4.2 HS Differential Transmitter

The HS transmitter is always operated on the UTMI parallel interface. The parallel data on the interface is serialized, bit stuffed, NRZI encoded, and transmitted as a dc output current on DP or DM, depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double, thereby doubling the differential amplitude seen on the DP/DM lines.

Table 7-6 lists the characteristics of the HS differential transmitter.

Table 7-6. HS Differential Transmitter

Parameter		Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Output Levels for HS						
HS TX idle level	V _{HSOI}	Absolute voltage DP/DM – internal/external 45 Ω	–10	0	10	mV
HS TX data signaling high	V _{HSOH}	Absolute voltage DP/DM – internal/external 45 Ω	360	400	440	mV
HS data signaling low	V _{HSOL}		–10	0	10	mV
Chirp J level	V _{CHIRPJ}	Differential voltage	700	800	1100	mV
Chirp K level	V _{CHIRPK}	Differential voltage	–900	–800	–500	mV
HS TX disconnect threshold	V _{DISCOUT}	Absolute voltage DP/DM – no external 45 Ω	700			mV
Driver Characteristics						
Rise time	t _{HSR}	(10%–90%)	500			ps
Fall time	t _{HSF}	(10%–90%)	500			ps
Driver output resistance	Z _{HSDRV}	Also serves as HS termination	40.5	45	49.5	Ω

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

7.1.4.3 CEA/UART Driver

Table 7-7 lists the characteristics of the CEA/UART driver.

Table 7-7. CEA/UART Driver

Parameter		Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
UART Driver CEA						
Phone UART edge rates	t _{PH_UART_EDGE}	DP_PULLDOWN asserted			1	μs
Serial interface output high	V _{OH_SER}	ISOURCE = 4 mA	2.4	3.3	3.6	V
Serial interface output low	V _{OL_SER}	ISINK = –4 mA	0	0.1	0.4	V
Carkit Pulse Driver						
Pulse match tolerance	QPLS_MTCH	ZCR_SPKR_IN = 60 kΩ at f = 1 kHz			5%	
Phone D– interrupt pulse width	t _{PH_PLS_POS}	ZCR_SPKR_IN = 60 kΩ at f = 1 kHz	200		600	ns
Phone positive pulse voltage	V _{PH_PLS_POS}	ZCR_SPKR_IN = 60 kΩ at f = 1 kHz	2.8		3.6	V

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

7.1.4.4 Pullup/Pulldown Resistors

Table 7-8 lists the characteristics of pullup/pulldown resistors.

Table 7-8. Pullup/Pulldown Resistors

Parameter		Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Pullup Resistors						
Bus pullup resistor on upstream port (idle bus)	R _{PUI}	Bus idle	0.9	1.1	1.575	kΩ
Bus pullup resistor on upstream port (receiving)	R _{PUA}	Bus driven/driver outputs unloaded	1.425	2.2	3.09	
High (floating)	V _{IHZ}	Pullups/pulldowns on DP and DM lines	2.7		3.6	V
Phone D+ pullup voltage	V _{PH_DP_UP}	Driver outputs unloaded	3	3.3	3.6	V
Pulldown Resistors						
Phone D+/- pulldown	R _{PH_DP_DWN}	Driver outputs unloaded	14.25	18	24.8	kΩ
	R _{PH_DM_DWN}					
High (floating)	V _{IHZ}	Pullups/pulldowns on DP and DM lines	2.7		3.6	V
D+/- Data Line						
Upstream facing port	C _{INUB}	[1.0]		22	75	pF
OTG device leakage	V _{OTG_DATA_LKG}	[2]			0.342	V
Input impedance exclusive of pullup/pulldown ⁽⁴⁾	Z _{INP}	Driver outputs unloaded (waiver from USB.ORG Standard Committee)	80	120		kΩ

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Waiver received from usb.org standards committee on ZINP 300kmin specification

7.1.5 OTG Electrical Characteristics

The OTG block integrates three main functions:

- The USB plug detection function on VBUS and ID
- The ID resistor detection
- The VBUS level detection

7.1.5.1 OTG VBUS Electrical Characteristics

Table 7-9 lists the electrical characteristics of the OTG VBUS.

Table 7-9. OTG VBUS Electrical Characteristics

Parameter		Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
VBUS Wake-Up Comparator						
VBUS wake-up delay	DEL _{VBUS_WK_UP}				15	μs
VBUS wake-up threshold	V _{VBUS_WK_UP}		0.5	0.6	0.7	V
VBUS Comparators						
A-device session valid	V _{A_SESS_VLD}		0.8	1.1	1.4	V
A-device V _{BUS} valid	V _{A_VBUS_VLD}		4.4	4.5	4.6	V
B-device session end	V _{B_SESS_END}		0.2	0.5	0.8	V
B-device session valid	V _{B_SESS_VLD}		2.1	2.4	2.7	V
VBUS Line						
A-device V _{BUS} input impedance to ground	R _{A_BUS_IN}	SRP (V _{BUS} pulsing) capable A-device not driving V _{BUS}			100	kΩ
B-device V _{BUS} SRP pulldown	R _{B_SRP_DWN}	5.25 V/8 mA, pullup voltage = 3 V	0.656	10		kΩ
B-device V _{BUS} SRP pullup	R _{B_SRP_UP}	(5.25 V – 3 V)/8 mA, pullup voltage = 3 V	0.281	1	2	kΩ
B-device V _{BUS} SRP rise time maximum for OTG-A communication	t _{RISE_SRP_UP_Max}	0 to 2.1 V with < 13 μF load			36	ms
B-device V _{BUS} SRP rise time minimum for standard host connection	t _{RISE_SRP_UP_Min}	0.8 to 2.0 V with > 97 μF load	60			ms
VBUS line maximum voltage		If VBUS_CHRG bit is low			6	V

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

7.1.5.2 OTG ID Electrical Characteristics

Table 7-10 lists the electrical characteristics of OTG ID.

Table 7-10. OTG ID Electrical Characteristics

Parameter		Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
ID Wake-Up Comparator						
ID wake-up comparator	R _{ID_WK_UP}	Wake-up when ID shorted to ground through a resistor lower than 445 kΩ (±1%)	445			kΩ
ID Comparators — ID External Resistor Specifications						
ID ground comparator	R _{ID_GND}	ID_GND interrupt when ID shorted to ground through a resistor lower than 10 Ω	0	5	10	Ω
ID 100k comparators	R _{ID_100K}	ID_100K interrupt when 102 kΩ (1%) resistor plugged in	101	102	103	kΩ
ID 200k comparators	R _{ID_200K}	ID_200K interrupt when 200 kΩ (1%) resistor plugged in	198	200	202	kΩ
ID 440k comparators	R _{ID_440K}	ID_440K interrupt when 440 kΩ (1%) resistor plugged in	435	440	445	kΩ
ID Float comparator	R _{ID_FLOAT}	ID_FLOAT interrupt when ID shorted to ground through a resistor higher than 560 kΩ	1400			kΩ
ID Line						
Phone I _D pullup to V _{PH_ID_UP}	R _{PH_ID_UP}	ID unloaded (V _{RUSB})	70	200	286	kΩ

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

Table 7-10. OTG ID Electrical Characteristics (continued)

Parameter		Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Phone I _D pullup voltage	VPH_ID_UP	Connected to VRUSB	2.5		3.2	V
ID line maximum voltage					5.25	V

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8 MADC

8.1 General Description

The TPS65920/TPS65930 device provides the MADC resource to the host processors in the system (hardware and software conversion modes).

The MADC generates interrupt signals to the host processors. Interrupts are handled primarily by the MADC internal secondary interrupt handler and secondly at the upper level (outside the MADC) by the TPS65920/TPS65930 interrupt primary handler.

8.2 MADC Electrical Characteristics

Table 8-1 lists the electrical characteristics of the MADC.

Table 8-1. MADC Electrical Characteristics

Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Resolution			10		Bit
ADIN2 input dynamic range for external input		0		2.5	V
MADC voltage reference			1.5		V
ADIN0 differential nonlinearity		–1		1	LSB
ADIN0 integral nonlinearity	Best fitting	–2		2	LSB
Integral nonlinearity for ADIN2	Best fitting for codes 230 to maximum	–2		2	LSB
	Best fitting considering offset of 25 LSB	–3.75		3.75	LSB
Offset	Best fitting	–28.5		28.5	mV
Input bias			1		μA
Input capacitor C _{BANK}				10	pF
Maximum source input resistance R _s (for all 16 internal or external inputs)				100	kΩ
Input current leakage (for all 16 internal or external inputs)				1	μA

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

8.3 Channel Voltage Input Range

Table 8-2 lists the analog input voltage minimum and maximum values.

Table 8-2. Analog Input Voltage Range

Channel	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit	Prescaler
ADIN0: General-purpose input	0		1.5	V	No prescaler DC current source for battery identification through external resistor (10 μ A typical)
ADIN2: General-purpose input ⁽⁴⁾	0		2.5	V	Prescaler in the MADC to be in range 0 to >1.5 V

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) General-purpose inputs must be tied to ground when TPS65920/TPS65930 internal power supplies (VINTANA1 and VINTANA2) are off.

8.3.1 Sequence Conversion Time (Real-Time or Nonaborted Asynchronous)

Table 8-3 lists the sequence conversion timing characteristics.

Table 8-3. Sequence Conversion Timing Characteristics

Parameter	Comments	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
F	Running frequency		1		MHz
T = 1/F	Clock period		1		μ s
N	Number of analog inputs to convert in a single sequence	0		2	
Tstart	SW1, SW2, or USB asynchronous request or real-time STARTADC request	3		4	μ s
Tsettling time	Settling time to wait before sampling a stable analog input (capacitor bank charge time) Tsettling is calculated from the $\max((R_s + R_{on}) \cdot C_{bank})$ of the two possible input sources (internal or external). R_{on} is the resistance of the selection analog input switches (5 k Ω). This time is software-programmable by the open-core protocol (OCP) register.	5	12	20	μ s
Tstartsar	The successive approximation registers ADC start time		1		μ s
Tadc time	The successive approximation registers ADC conversion time		10		μ s
Tcapture time	Tcapture time is the conversion result capture time.		2		μ s
Tstop		1		2	μ s
Full-conversion sequence time	One channel (N = 1) ⁽⁴⁾	22		39	μ s
	Both channels ⁽⁴⁾	352		624	
Conversion sequence time	Without Tstart and Tstop: One channel (N = 1) ⁽⁴⁾	18		33	μ s
	Without Tstart and Tstop: Both channels ⁽⁴⁾	288		528	
STARTADC pulse duration	STARTADC period is T.	0.33		24	μ s

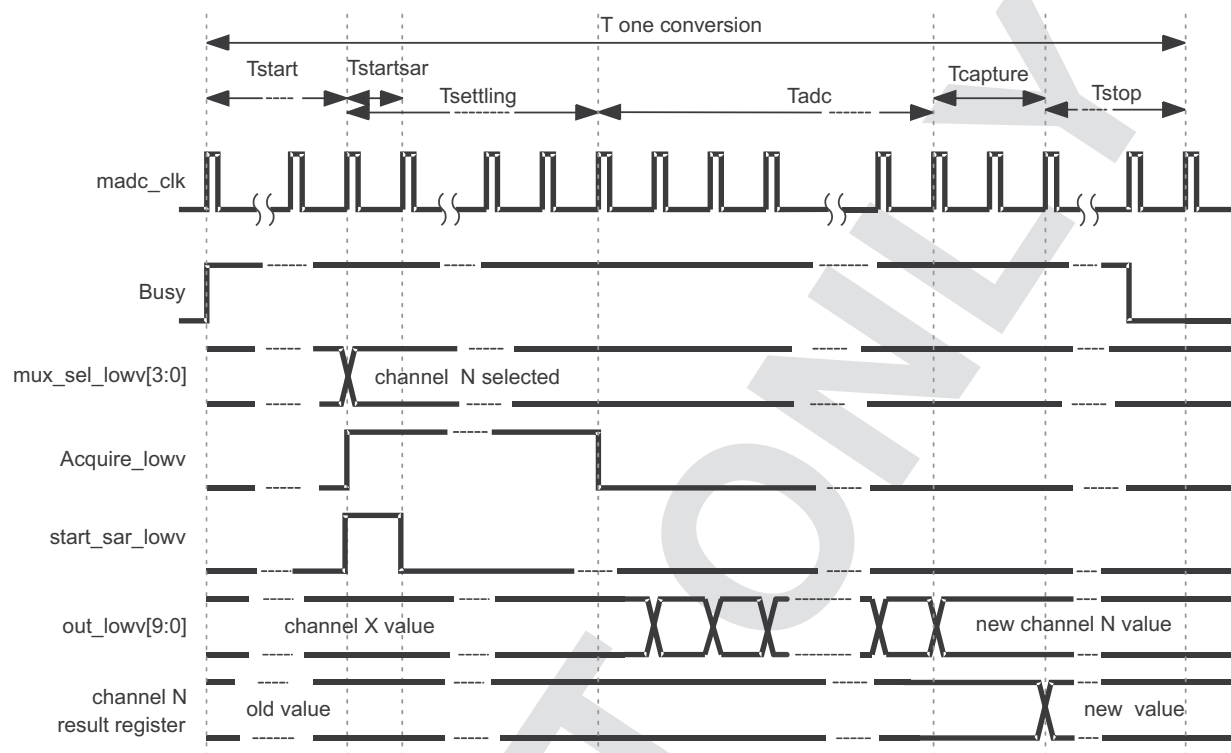
(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Total sequence conversion time general formula: $T_{start} + N \cdot (1 + T_{settling} + T_{adc} + T_{capture}) + T_{stop}$

Table 8-3 is illustrated in Figure 8-1, which is a conversion sequence general timing diagram. The *Busy* parameter indicates that a conversion sequence is running, and the *channel N result register* parameter corresponds to the result register of the RT/GP selected channel.



037-046

Figure 8-1. Conversion Sequence General Timing Diagram

9 LED Drivers

9.1 General Description

Two arrays of parallel LEDs are driven (dedicated for the phone light). The parallel LEDs are supplied by VBAT, and the external resistor value is given for each LED. The TPS65920/TPS65930 device supports two open-drain LED drivers for the keypad backlight, having drain connections tolerant of the main battery voltage.

Figure 9-1 is the LED driver block diagram. Table 9-1 lists the electrical characteristics of the LED driver.

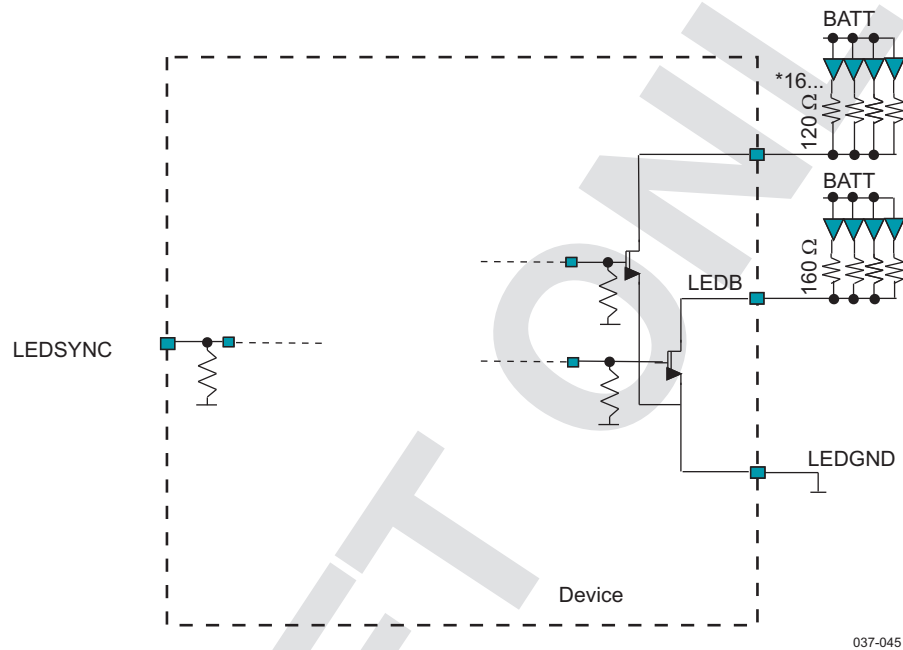


Figure 9-1. LED Driver Block Diagram

NOTE

For the component values, see Table 14-1.

Table 9-1. LED Driver Electrical Characteristics

Parameter	Conditions	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽²⁾	Unit
SW On resistance	$I_O = 160 \text{ mA}$		3	4	Ω
	$I_O = 60 \text{ mA}$		10	12	

(1) Min = Minimum value

(2) Max = Maximum value

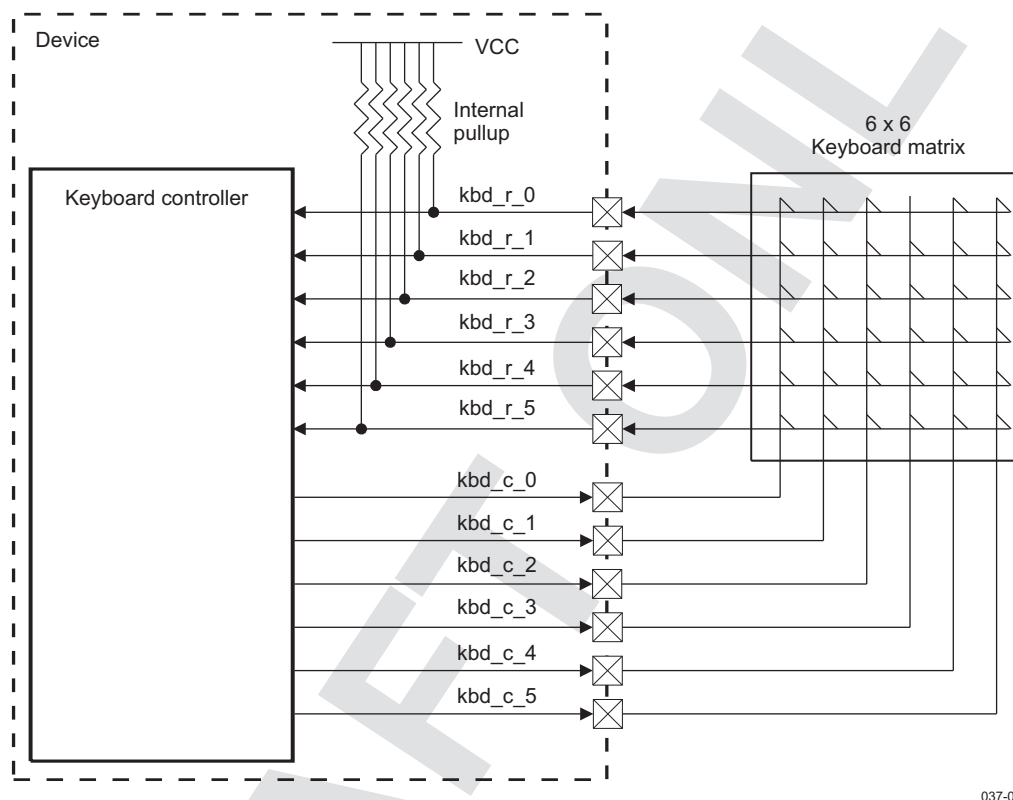
10 Keyboard

10.1 Keyboard Connection

The keyboard is connected to the chip using:

- KBR (5:0) input pins for row lines
- KBC (5:0) output pins for column lines

Figure 10-1 shows the keyboard connection.



037-014

Figure 10-1. Keyboard Connection

When a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted together. To allow key press detection, all input pins (KBR) are pulled up to V_{CC} and all output pins (KBC) are driven to a low level.

Any action on a button generates an interrupt to the sequencer.

The decoding sequence is written to allow detection of simultaneous press actions on several key buttons.

The keyboard interface can be used with a smaller keyboard area than 6×6 . To use a 3×3 keyboard, KBR(4) and KBR(5) must be tied high to prevent any scanning process distribution.

11 Clock Specifications

The TPS65920/TPS65930 device includes several I/O clock pins. The TPS65920/TPS65930 device has two sources of high-stability clock signals: the external high-frequency clock (HFCLKIN) input and an onboard 32-kHz oscillator (an external 32-kHz signal can be provided). Figure 11-1 is the clock overview.

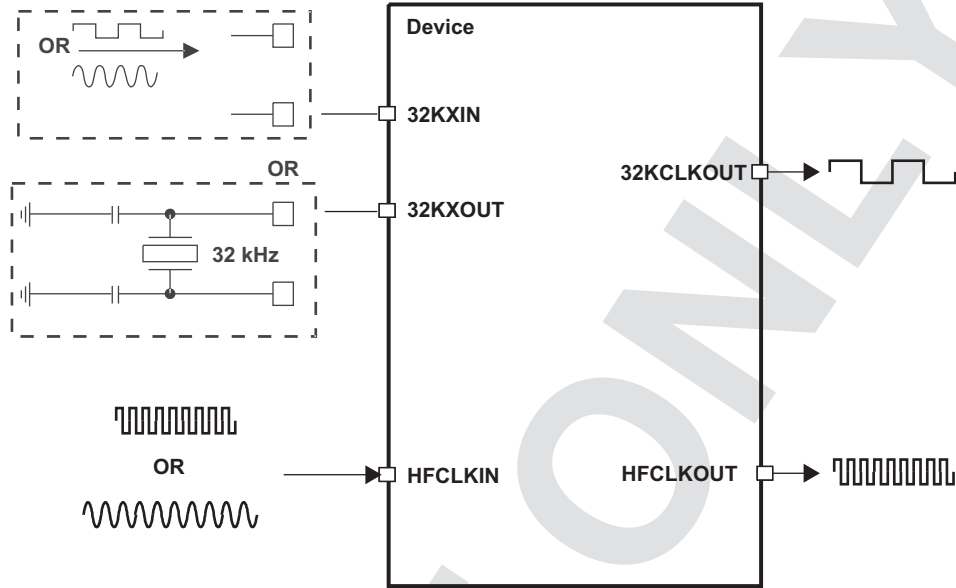


Figure 11-1. Clock Overview

11.1 Clock Features

The TPS65920/TPS65930 device accepts two sources of high-stability clock signals:

- 32KXIN/32KXOUT: Onboard 32-kHz crystal oscillator (an external 32-kHz input clock can be provided)
- HFCLKIN: External high-frequency clock (19.2, 26, or 38.4 MHz).

The TPS65920/TPS65930 device can provide:

- 32KCLKOUT digital output clock
- HFCLKOUT digital output clock with the same frequency as the HFCLKIN input clock

11.2 Input Clock Specifications

The clock system accepts two input clock sources:

- 32-kHz crystal oscillator clock or sinusoidal/squared clock
- HFCLKIN high-frequency input clock

11.2.1 Clock Source Requirements

Table 11-1 lists the input clock requirements.

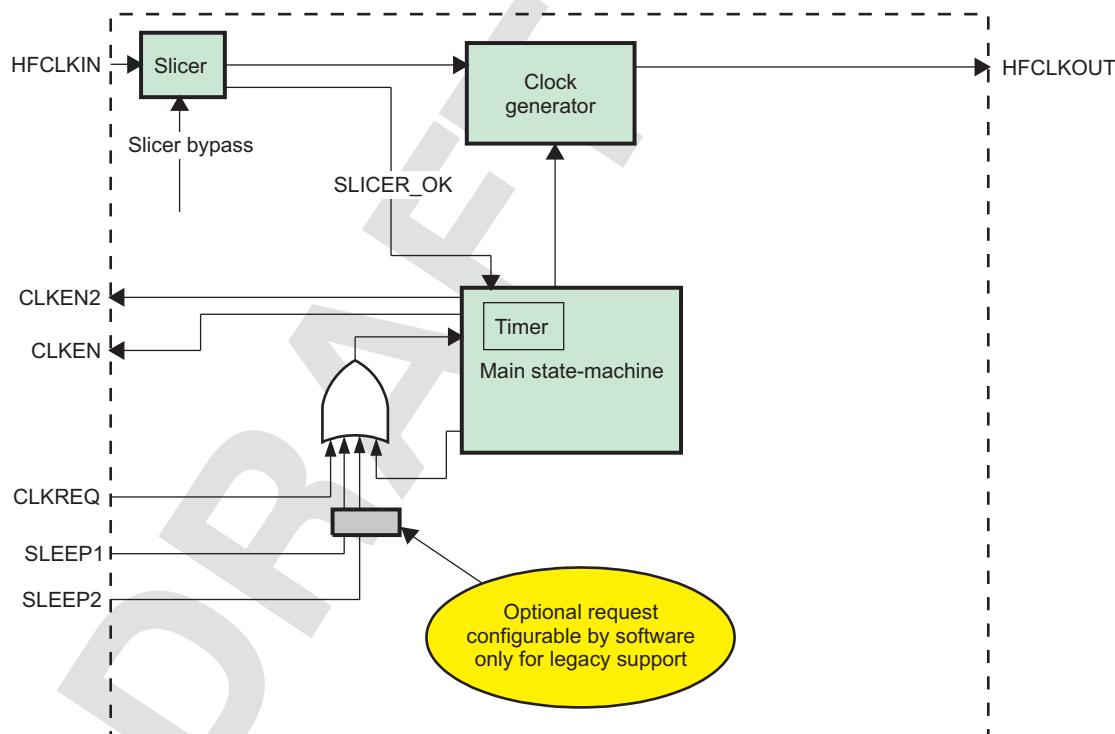
Table 11-1. TPS65920/TPS65930 Input Clock Source Requirements

Pad	Clock Frequency		Stability	Duty Cycle
32KXIN 32KXOUT	32.768 kHz	Crystal	± 30 ppm	40%/60%
		Square wave	–	45%/55%
		Sine wave	–	–
HFCLKIN	19.2, 26, 38.4 MHz	Square wave	± 150 PPM	45%/55%
		Sine wave	–	–

11.2.2 HFCLKIN

HFCLKIN can be a square- or a sine-wave input clock. If a square-wave input clock is provided, it is recommended to switch the block to bypass mode to avoid loading the clock.

Figure 11-2 shows the HFCLKIN clock distribution.



037-044

Figure 11-2. HFCLKIN Clock Distribution

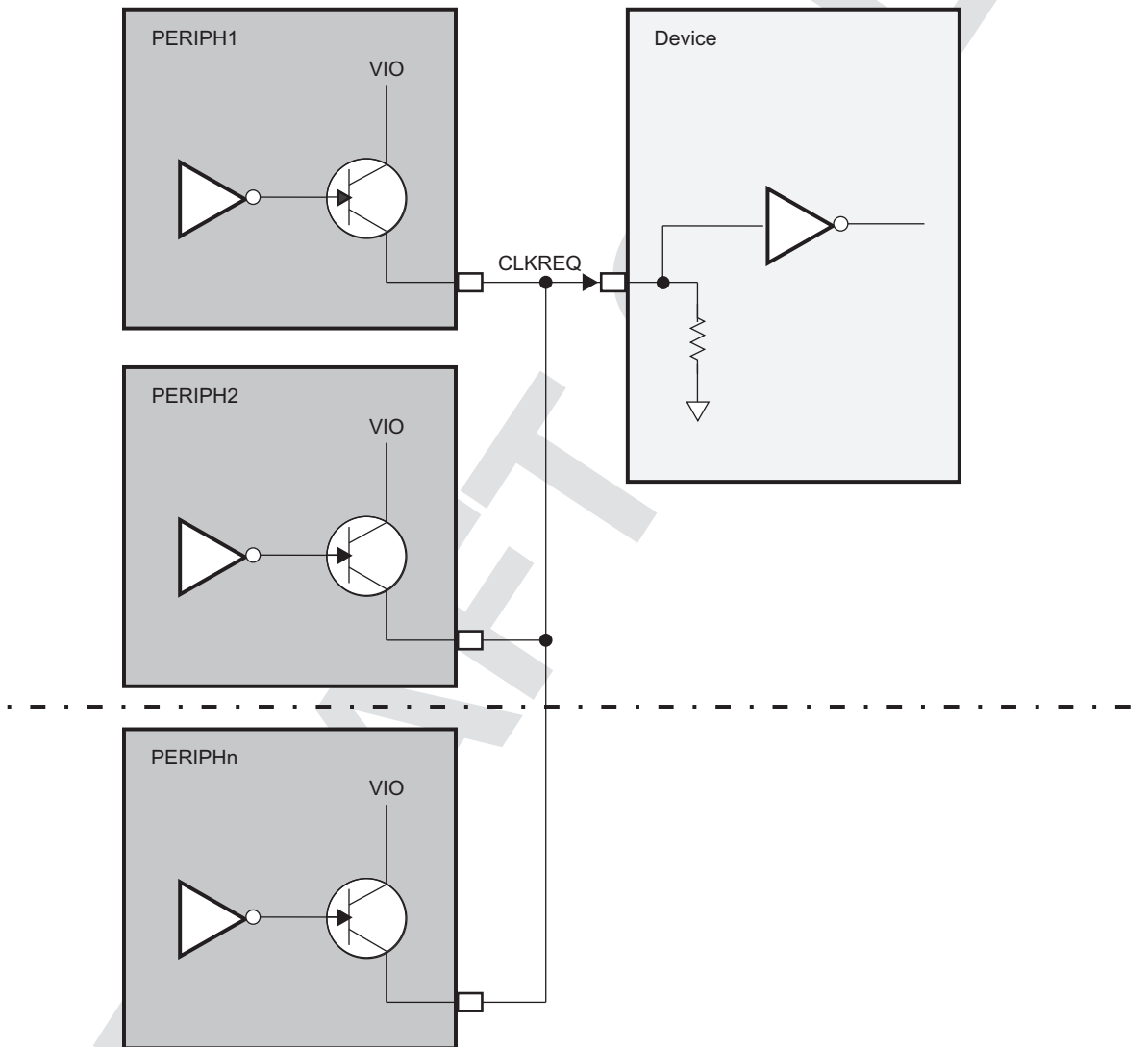
When a device needs a clock signal other than 32.768 kHz, it makes a clock request and activates the CLKREQ pin. As a result, the TPS65920/TPS65930 device immediately sets CLKEN to 1 to warn the

clock provider in the system about the clock request and starts a timer (maximum of 5.2 ms using the 32.768-kHz clock). When the timer expires, the TPS65920/TPS65930 device opens a gated clock, the timer automatically reloads the defined value, and a high-frequency output clock signal is available through the HFCLKOUT pin. The output drive of HFCLKOUT is programmable (minimum load 10 pF, maximum load 40 pF) and must be at 40 pF by default.

With a register setting, the mirroring of CLKEN can be enabled on CLKEN2. When this mirroring feature is not enabled, CLKEN2 can be used as a general-purpose output controlled through I²C accesses.

CLKREQ, when enabled, has a weak pulldown resistor to support the wired-OR clock request.

Figure 11-3 shows an example of the wired-OR clock request.



037-043

Figure 11-3. Example of Wired-OR Clock Request

The timer default value must be the worst case (10 ms) for the clock providers. For legacy or workaround support, the NSLEEP1 and NSLEEP2 signals can also be used as a clock request even if it is not their primary goal. By default, this feature is disabled and must be enabled individually by setting the register bits associated with each signal.

When the external clock signal is present on the HFCLKIN ball, it is possible to use this clock instead of the internal RC oscillator and then synchronize the system on the same clock. The RC oscillator can then go to idle mode.

Table 11-2 lists the input clock electrical characteristics of the HFCLKIN input clock.

Table 11-2. HFCLKIN Input Clock Electrical Characteristics

Parameter Description	Configuration Mode Slicer	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Frequency		19.2, 26, or 38.4			MHz
Start-up time	LP ⁽⁴⁾ /HP ⁽⁵⁾ (sine wave)			4	μs
Input dynamic range	LP/HP (sine wave)	0.3	0.7	1.45	V _{PP}
	BP ⁽⁶⁾ /PD ⁽⁷⁾ (square wave)	0		1.85 ⁽⁸⁾	
Current consumption	LP			175	μA
	HP			235	
	BP/PD			39	nA
Harmonic content of input signal (with 0.7-V _{PP} amplitude): second component	LP/HP (sine wave)			–25	dBc
V _{IH} Voltage input high	BP (square wave)	1			V
V _{IL} Voltage input low	BP (square wave)			0.6	V

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) LP = Low-power mode

(5) HP = High-power mode

(6) BP = Bypass mode

(7) PD = Power-down mode

(8) Bypass input max voltage is the same as the maximum voltage provided for the I/O interface (IO.1P8V).

Table 11-3 lists the input clock timing requirements of the HFCLKIN input clock when the source is a square wave. Figure 11-4 shows the HFCLKIN squared input clock timings.

Table 11-3. HFCLKIN Square Input Clock Timing Requirements with Slicer in Bypass

Name	Parameter	Description	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
CH0	1/t _C (HFCLKIN)	Frequency, HFCLKIN	19.2, 26, or 38.4			MHz
CH1	t _W (HFCLKIN)	Pulse duration, HFCLKIN low or high	0.45*t _C (HFCLKIN)		0.55*t _C (HFCLKIN)	ns
CH3	t _R (HFCLKIN)	Rise time, HFCLKIN ⁽⁴⁾			0.05*t _C (HFCLKIN)	ns
CH4	t _F (HFCLKIN)	Fall time, HFCLKIN ⁽⁴⁾			0.05*t _C (HFCLKIN)	ns

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) The capacitive load is 30 fF.

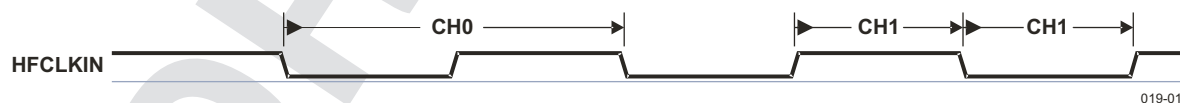


Figure 11-4. HFCLKIN Squared Input Clock

11.2.3 32-kHz Input Clock

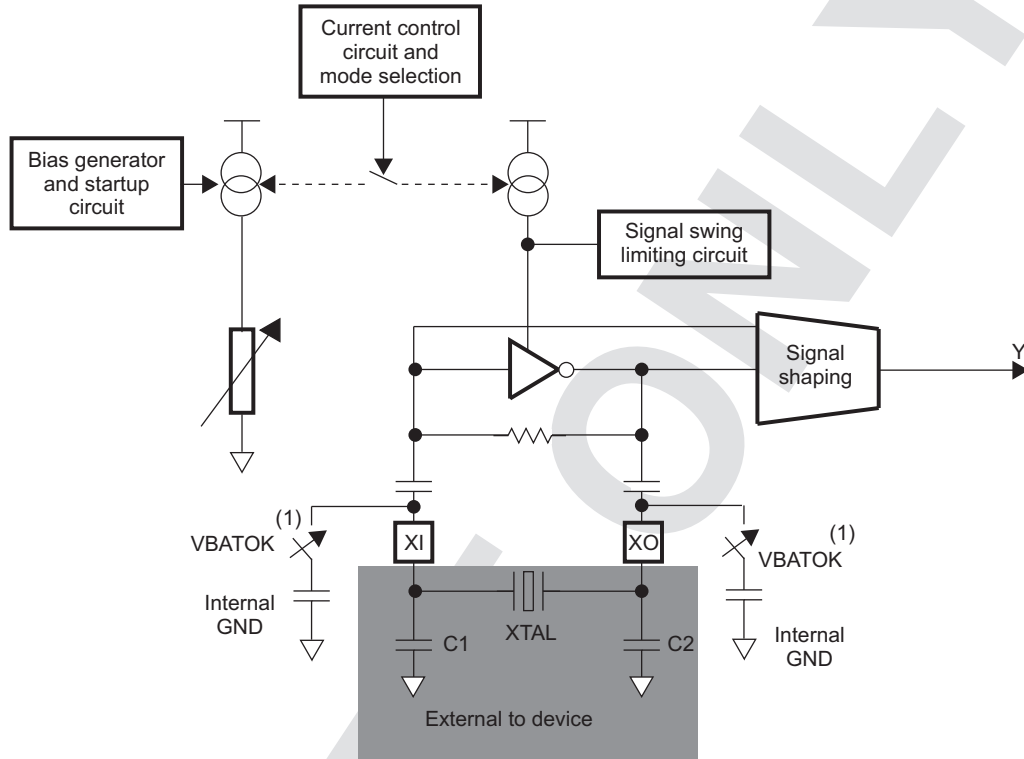
A 32.768-kHz input clock (often abbreviated to 32-kHz) generates the clocks for the RTC. It has a low-jitter mode where the current consumption increases for lower jitter. It is possible to use the 32-kHz input clock with an external crystal or clock source. Depending on the mode chosen, the 32K oscillator is configured one of two ways:

- An external 32.768-kHz crystal through the 32KXIN/32KXOUT balls (see Figure 11-5). This configuration is available only for master mode (for more information, see Section 12).

- An external square/sine wave of 32.768 kHz through 32KXIN with amplitude equal to 1.8 or 1.85 V (see [Figure 11-7](#), [Figure 11-8](#), and [Figure 11-9](#)). This configuration is available for the master and slave modes (for more information, see [Section 12](#)).

11.2.3.1 External Crystal Description

[Figure 11-5](#) shows the 32-kHz oscillator block diagram with crystal in master mode.



037-042

NOTE: Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

Figure 11-5. 32-kHz Oscillator Block Diagram In Master Mode With Crystal

CXIN and CXOUT represent the total capacitance of the printed circuit board (PCB) and components, excluding the crystal. Their values depend on the datasheet of the crystal, the internal capacitors, and the parallel capacitor. The frequency of the oscillations depends on the value of the capacitors. The crystal must be in the fundamental mode of operation and parallel resonant.

NOTE

For the values of CXIN and CXOUT, see [Table 14-1](#).

[Table 11-4](#) lists the required electrical constraints.

Table 11-4. Crystal Electrical Characteristics

Parameter	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Parallel resonance crystal frequency		32.768		kHz
Input voltage, Vin (normal mode)	1.0	1.3	1.55	V
Internal capacitor on each input (Cint)		10		pF
Parallel input capacitance (Cpin)			1	pF

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

Table 11-4. Crystal Electrical Characteristics (continued)

Parameter	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
Nominal load cap on each oscillator input CXIN and CXOUT ⁽⁴⁾	CXIN = CXOUT = Cosc*2 – (Cint + Cpin)			pF
Pin-to-pin capacitance		1.6	1.8	pF
Crystal ESR ⁽⁵⁾			75	kΩ
Crystal shunt capacitance, C _O			1	pF
Crystal tolerance at room temperature, 25°C	–30		30	ppm
Crystal tolerance versus temperature range (–40°C to 85°C)	–200		200	ppm
Maximum drive power			1	μW
Operating drive level			0.5	μW

(4) Nominal load capacitor on each oscillator input defined as CXIN = CXOUT = Cosc*2 – (Cint + Cpin). Cosc is the load capacitor defined in the crystal oscillator specification, Cint is the internal capacitor, and Cpin is the parallel input capacitor.

(5) The crystal motional resistance R_m relates to the equivalent series resistance (ESR) by the following formula:

$$ESR = R_m \left(1 + \frac{C_O}{C_L} \right)^2$$

Measured with the load capacitance specified by the crystal manufacturer. If CXIN = CXOUT = 10 pF, C_L = 5 pF. Parasitic capacitance from the package and board must also be considered.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 11-5 and Table 11-6 list the switching characteristics of the oscillator and the timing requirements of the 32.768-kHz input clock. Figure 11-6 shows the crystal oscillator output in normal mode.

Table 11-5. Base Oscillator Switching Characteristics

Name	Parameter Description		Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
f _P	Oscillation frequency			32.768		kHz
t _{sx}	Start-up time				0.5	s
I _{DDA}	Active current consumption	LOJIT <1:0> = 00			1.8	μA
		LOJIT <1:0> = 11			8	
I _{DDQ}	Current consumption	Low battery mode (1.2 V)			1	μA
		Startup			8	

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

Table 11-6. 32-kHz Crystal Input Clock Timing Requirements

Name	Parameter Description		Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
OC0	1/t _{C(32KHZ)}	Frequency, 32 kHz		32.768		kHz
OC1	t _{W(32KHZ)}	Pulse duration, 32 kHz low or high	0.40*t _{C(32KHZ)}		0.60*t _{C(32KHZ)}	μs

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

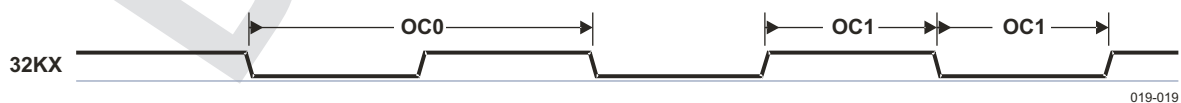
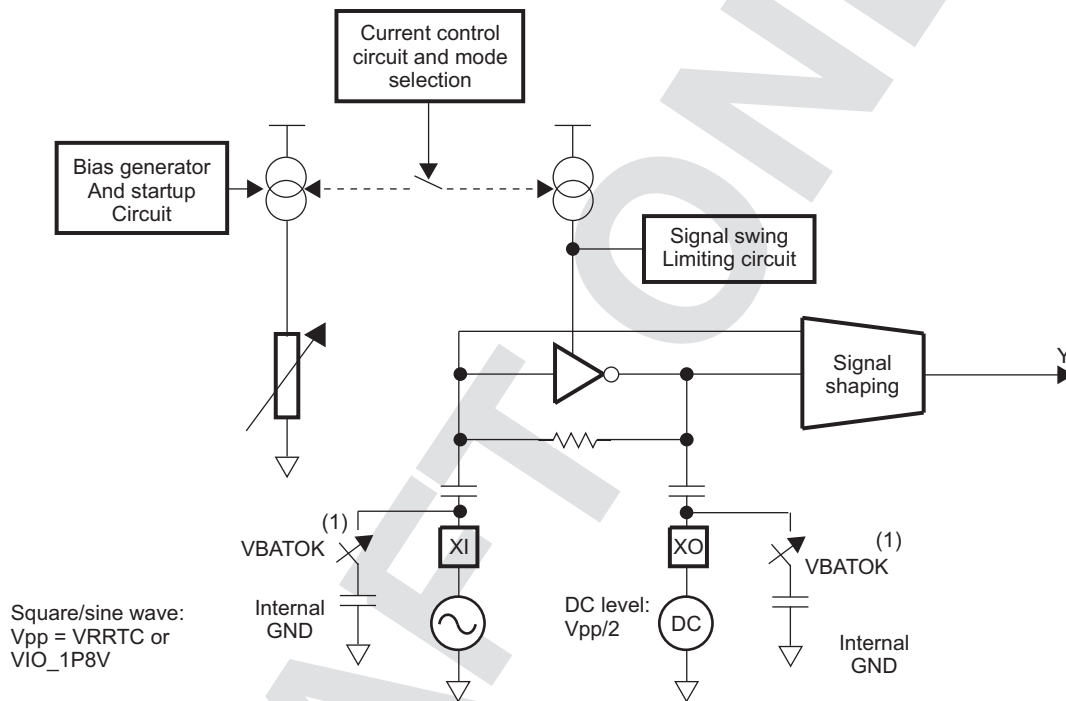


Figure 11-6. 32-kHz Crystal Input

11.2.3.2 External Clock Description

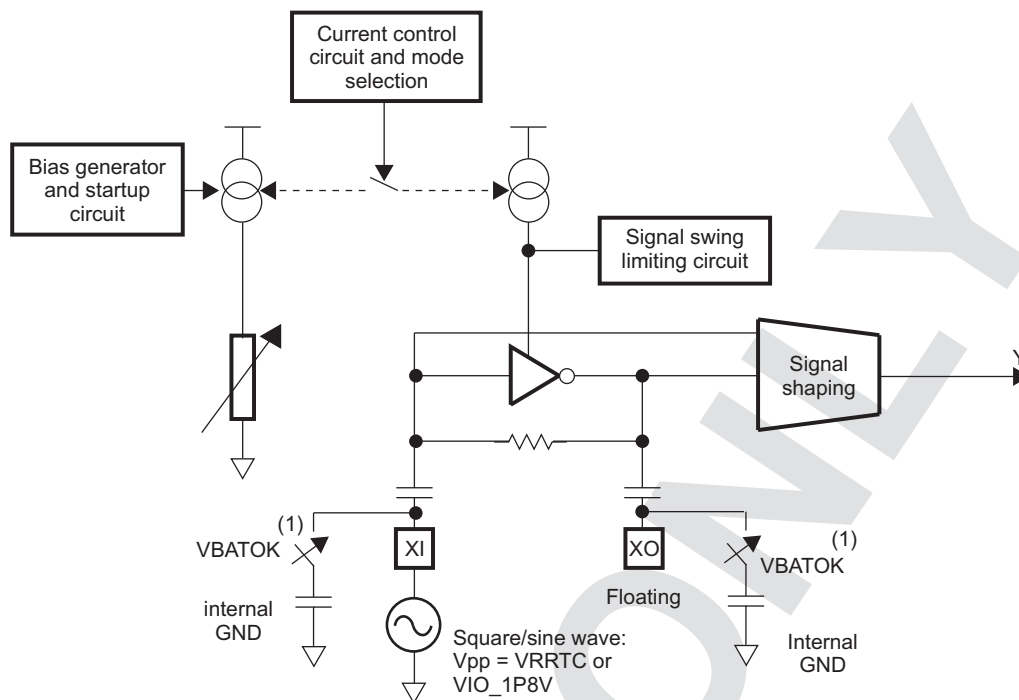
When an external 32K clock is used instead of a crystal, three configuration can be used:

- A square- or sine-wave input can be applied to the 32KXIN pin with amplitude of 1.85 or 1.8 V. The 32KXOUT pin can be driven to a dc value of the square- or sine-wave amplitude divided by 2. This configuration, shown in Figure 11-7, is recommended if a large load is applied on the 32KXOUT pin.
- A square- or sine-wave input can be applied to the 32KXIN pin with amplitude of 1.85 or 1.8 V. The 32KXOUT pin can be left floating. This configuration, showed in Figure 11-8, is used if no charge is applied on the 32KXOUT pin.
- The oscillator is in bypass mode and a square-wave input can be applied to the 32KXIN pin with amplitude of 1.8 V. The 32KXOUT pin can be left floating. This configuration, shown in Figure 11-9, is used if the oscillator is in bypass mode.



(1) Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

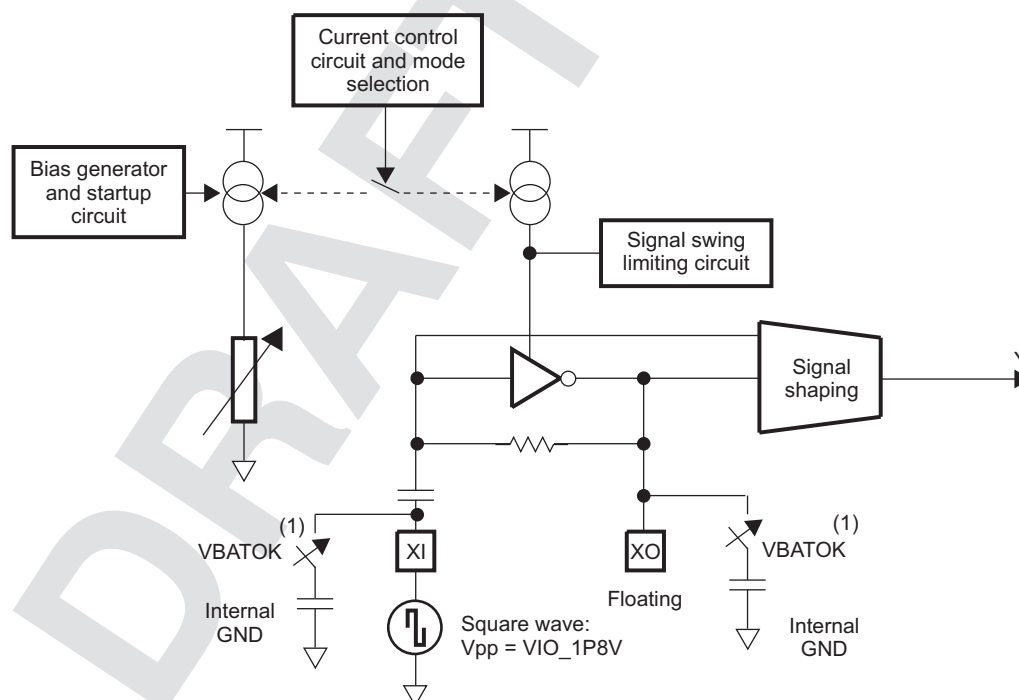
Figure 11-7. 32-kHz Oscillator Block Diagram Without Crystal Option 1



037-039

- (1) Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

Figure 11-8. 32-kHz Oscillator Block Diagram Without Crystal Option 2



037-040

- (1) Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

Figure 11-9. 32-kHz Oscillator in Bypass Mode Block Diagram Without Crystal Option 3

Table 11-7 lists the electrical constraints required by the 32-kHz input square- or sine-wave clock.

Table 11-7. 32-kHz Input Square- or Sine-Wave Clock Source Electrical Characteristics

Name	Parameter Description	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
f	Frequency		32.768		kHz
C _I	Input capacitance		35		pF
C _{FI}	On-chip foot capacitance to GND on each input (see Figure 11-7, Figure 11-8, and Figure 11-9)		10		pF
V _{PP}	Square-/sine-wave amplitude in bypass mode or not		1.8 ⁽⁴⁾		V
V _{IH}	Voltage input high, square wave in bypass mode	0.8			V
V _{IL}	Voltage input low, square wave in bypass mode			0.6	V

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) Bypass input maximum voltage is the same as the maximum voltage provided for the I/O interface.

Table 11-8 lists the timing requirements of the 32-kHz square-wave input clock.

Table 11-8. 32-kHz Square-Wave Input Clock Source Timing Requirements

Name	Parameter	Description	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
CK0	1/t _{C(32KHZ)}	Frequency, 32 kHz		32.768		MHz
CK1	t _{W(32KHZ)}	Pulse duration, 32 kHz low or high	0.45*t _{C(32KHZ)}		0.55*t _{C(32KHZ)}	μs
CK3	t _{R(32KHZ)}	Rise time, 32 kHz ⁽⁴⁾			0.1*t _{C(32KHZ)}	μs
CK4	t _{F(32KHZ)}	Fall time, 32 kHz ⁽⁴⁾			0.1*t _{C(32KHZ)}	μs

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) The capacitive load is 30 pF.

Figure 11-10 shows the 32-kHz square- or sine-wave input clock.

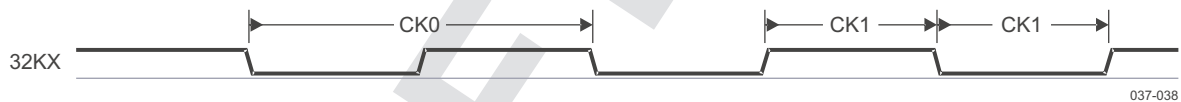


Figure 11-10. 32-kHz Square- or Sine-Wave Input Clock

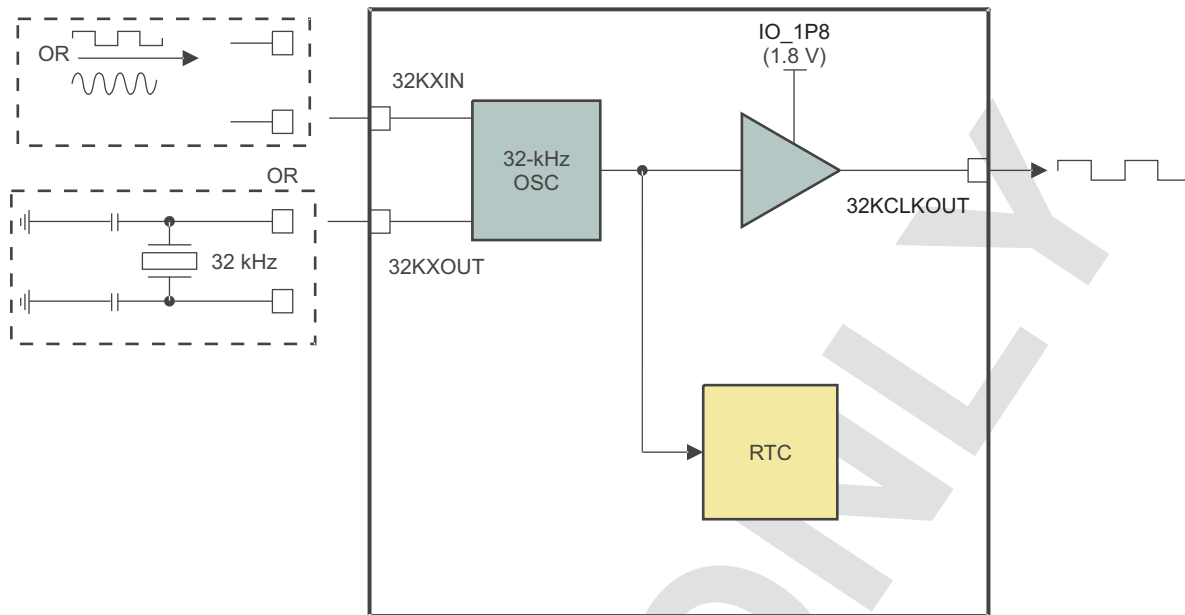
11.3 Output Clock Specifications

The TPS65920/TPS65930 device provides two output clocks:

- 32KCLKOUT
- HFCLKOUT

11.3.1 32KCLKOUT Output Clock

Figure 11-11 is the block diagram for the 32.768-kHz clock output.



037-037

Figure 11-11. 32.768-kHz Clock Output Block Diagram

The TPS65920/TPS65930 device has an internal 32.768-kHz oscillator connected to an external 32.768-kHz crystal through the 32KXIN/32KXOUT balls or an external digital 32.768-kHz clock through the 32KXIN input (see [Figure 11-11](#)). The TPS65920/TPS65930 device also generates a 32.768-kHz digital clock through the 32KCLKOUT pin and can broadcast it externally to the application processor or any other devices. The 32KCLKOUT clock is broadcast by default in TPS65920/TPS65930 active mode, but can be disabled if it is not used.

The 32.768-kHz clock (or signal) is also used to clock the RTC embedded in the TPS65920/TPS65930 device. The RTC is not enabled by default. The host processor must set the correct date and time and enable the RTC functionality.

The 32KCLKOUT output buffer can drive several devices (up to 40-pF load). At startup, 32KCLKOUT must be stabilized (frequency/duty cycle) before the signal output. Depending on the startup conditions, this can delay the startup sequence.

[Table 11-9](#) lists the electrical characteristics of the 32KCLKOUT output clock.

Table 11-9. 32KCLKOUT Output Clock Electrical Characteristics

Name	Parameter Description	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
f	Frequency		32.768		kHz
C _L	Load capacitance			40	pF
V _{OUT}	Output clock voltage, depending on output reference level IO_1P8 (see Section 2)		1.8 ⁽⁴⁾		V
V _{OH}	Voltage output high	V _{OUT} – 0.45		V _{OUT}	V
V _{OL}	Voltage output low	0		0.45	V

(1) Min = Minimum value

(2) Typ = Typical value

(3) Max = Maximum value

(4) The output voltage depends on the output reference level, which is IO_1P8 (see [Section 2, Terminal Description](#)).

[Table 11-10](#) lists the output clock switching characteristics. [Figure 11-12](#) shows the 32KCLKOUT output clock waveform.

Table 11-10. 32KCLKOUT Output Clock Switching Characteristics

Name	Parameter	Description	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
CK0	$1/t_{C(32KCLKOUT)}$	Frequency		32.768		MHz
CK1	$t_{W(32KCLKOUT)}$	Pulse duration, 32KCLKOUT low or high	$0.40 \cdot t_{C(32KCLKOUT)}$		$0.60 \cdot t_{C(32KCLKOUT)}$	ns
CK2	$t_{R(32KCLKOUT)}$	Rise time, 32KCLKOUT ⁽⁴⁾			16	ns
CK3	$t_{F(32KCLKOUT)}$	Fall time, 32KCLKOUT ⁽⁴⁾			16	ns

- (1) Min = Minimum value
(2) Typ = Typical value
(3) Max = Maximum value
(4) The output capacitive load is 30 pF.



Figure 11-12. 32KCLKOUT Output Clock

11.3.2 HFCLKOUT Output Clock

Table 11-11 lists the electrical characteristics of the HFCLKOUT output clock.

Table 11-11. HFCLKOUT Output Clock Electrical Characteristics

Name	Parameter Description	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
f	Frequency		19.2, 26, or 38.4		MHz
C _L	Load capacitance			30	pF
V _{OUT}	Output clock voltage, depending on output reference level IO_1P8 (see Section 2)		1.8 ⁽⁴⁾		V
V _{OH}	Voltage output high	$V_{OUT} - 0.45$		V_{OUT}	V
V _{OL}	Voltage output low	0		0.45	V

- (1) Min = Minimum value
(2) Typ = Typical value
(3) Max = Maximum value
(4) The output voltage depends on the output reference level, which is IO_1P8 (see Section 2).

Table 11-12 lists the switching characteristics of the HFCLKOUT output clock.

Table 11-12. HFCLKOUT Output Clock Switching Characteristics

Name	Parameter	Description	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽³⁾	Unit
CHO1	$1/t_{C(HFCLKOUT)}$	Frequency		19.2, 26, or 38.4		MHz
CHO2	$t_{W(HFCLKOUT)}$	Pulse duration, HFCLKOUT low or high	$0.40 \cdot t_{C(HFCLKOUT)}$		$0.60 \cdot t_{C(HFCLKOUT)}$	ns
CHO3	$t_{R(HFCLKOUT)}$	Rise time, HFCLKOUT ⁽⁴⁾			2.6	ns
CHO4	$t_{F(HFCLKOUT)}$	Fall time, HFCLKOUT ⁽⁴⁾			2.6	ns

- (1) Min = Minimum value
(2) Typ = Typical value
(3) Max = Maximum value
(4) The output capacitive load is equivalent to 30 pF.

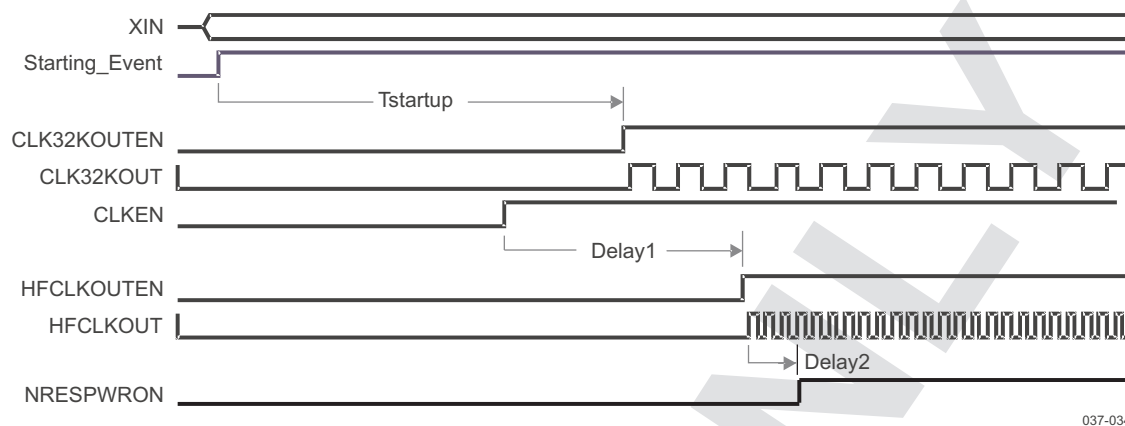
Figure 11-13 shows the HFCLKOUT output clock waveform.



Figure 11-13. HFCLKOUT Output Clock

11.3.3 Output Clock Stabilization Time

Figure 11-14 shows the 32KCLKOUT and HFCLKOUT clock stabilization time.

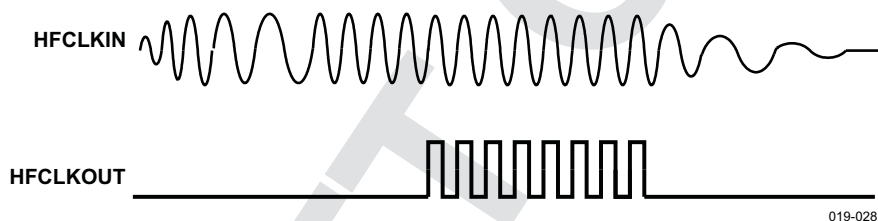


037-034

NOTE: Tstartup, Delay1, and Delay2 depend on the boot mode (see [Section 4.4, Power Management](#)).

Figure 11-14. 32KCLKOUT and HFCLKOUT Clock Stabilization Time

Figure 11-15 shows the HFCLKOUT behavior.



019-028

Figure 11-15. HFCLKOUT Behavior

12 Timing Requirements and Switching Characteristics

12.1 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies are abbreviated, as shown in [Table 12-1](#).

Table 12-1. Timing Parameters

Subscripts	
Symbol	Parameter
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
H	High
L	Low
V	Valid
IV	Invalid
AE	Active edge
FE	First edge
LE	Last edge
Z	High impedance

12.2 Target Frequencies

Table 12-2 assumes testing over the recommended operating conditions.

Table 12-2. TPS65920/TPS65930 Interface Target Frequencies

I/O Interface	Interface Designation		Target Frequency 1.5 V
SmartReflex inter-integrated circuit (I ² C™) General-purpose I ² C	I ² C	Slave HS mode	3.6 Mbps
		Slave fast-speed mode	400 Kbps
		Slave standard mode	100 Kbps
USB	USB	HS	480 Mbps
		FS	12 Mbps
		LS	1.5 Mbps
JTAG	Real/View® ICE tool		30 MHz
	XDS560 and XDS510 tools		30 MHz
	Lauterbach™ tool		30 MHz
TDM/inter-IC sound (I2S™)	I2S		$1/(64 * F_s)^{(1)}$
	Right-justified		$1/(64 * F_s)^{(1)}$
	Left-justified		$1/(64 * F_s)^{(1)}$
	TDM		$1/(128 * F_s)^{(1)}$
Voice/Bluetooth® pulse code modulation (PCM) interface	PCM		$1/(65 * F_s)^{(2)}$

(1) F_s = 8 to 48 kHz; 96 kHz for RX path only (TDM/I2S interface)

(2) F_s = 8 or 16 kHz (voice/Bluetooth PCM interface)

12.3 I²C Timing

The TPS65920/TPS65930 device provides two I²C HS slave interfaces (one for general-purpose and one for SmartReflex). These interfaces support standard mode (100 Kbps), fast mode (400 Kbps), and HS mode (3.4 Mbps). The general-purpose I²C module embeds four slave hard-coded addresses (ID1 = 48h, ID2 = 49h, ID3 = 4Ah, and ID4 = 4Bh). The SmartReflex I²C module uses one slave hard-coded address (ID5). The master mode is not supported.

Table 12-3 and Table 12-4 assume testing over the recommended operating conditions (see Figure 12-1).

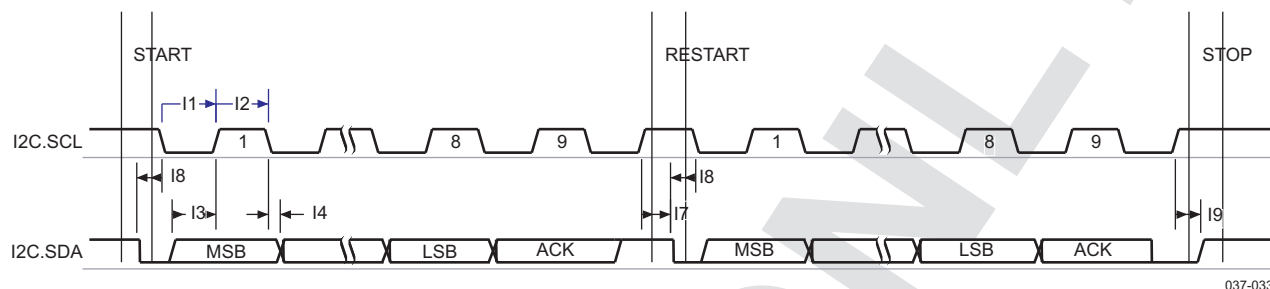


Figure 12-1. I²C Interface—Transmit and Receive in Slave Mode

Table 12-3. I²C Interface—Timing Requirements⁽¹⁾⁽²⁾

Notation	Parameter		Min ⁽³⁾	Max ⁽⁴⁾	Unit
Slave HS Mode					
I3	t _{su} (SDA-SCLH)	Setup time, SDA valid to SCL high	10		ns
I4	t _h (SCLL-SDA)	Hold time, SDA valid from SCL low	0	70	ns
I7	t _{su} (SCLH-SDAL)	Setup time, SCL high to SDA low	160		ns
I8	t _h (SDAL-SCLL)	Hold time, SCL low from SDA low	160		ns
I9	t _{su} (SDAH-SCLH)	Setup time, SDA high to SCL high	160		ns
Slave Fast-Speed Mode					
I3	t _{su} (SDA-SCLH)	Setup time, SDA valid to SCL high	100		ns
I4	t _h (SCLL-SDA)	Hold time, SDA valid from SCL low	0	0.9	ns
I7	t _{su} (SCLH-SDAL)	Setup time, SCL high to SDA low	0.6		ns
I8	t _h (SDAL-SCLL)	Hold time, SCL low from SDA low	0.6		ns
I9	t _{su} (SDAH-SCLH)	Setup time, SDA high to SCL high	0.6		ns
Slave Standard Mode					
I3	t _{su} (SDA-SCLH)	Setup time, SDA valid to SCL high	250		ns
I4	t _h (SCLL-SDA)	Hold time, SDA valid from SCL low	0		ns
I7	t _{su} (SCLH-SDAL)	Setup time, SCL high to SDA low	4.7		ns
I8	t _h (SDAL-SCLL)	Hold time, SCL low from SDA low	4		ns
I9	t _{su} (SDAH-SCLH)	Setup time, SDA high to SCL high	4		ns

(1) The input timing requirements are given by considering a rising or falling time of:

- 80 ns in HS mode (3.4 Mbps)
- 300 ns in fast-speed mode (400 Kbps)
- 1000 ns in standard mode (100 Kbps)

(2) SDA is equal to I2C.SR.SDA or I2C.CNTL.SDA.
SCL is equal to I2C.SR.SCL or I2C.CNTL.SCL.

(3) Min = Minimum value

(4) Max = Maximum value

Table 12-4 lists the switching requirements of the I²C interface.

Table 12-4. I²C Interface—Switching Requirements⁽¹⁾⁽²⁾

Notation	Parameter		Min ⁽³⁾	Max ⁽⁴⁾	Unit
Slave HS Mode					
I1	t _{w(SCLL)}	Pulse duration, SCL low	160		ns
I2	t _{w(SCLH)}	Pulse duration, SCL high	60		ns
Slave Fast-Speed Mode					
I1	t _{w(SCLL)}	Pulse duration, SCL low	1.3		ns
I2	t _{w(SCLH)}	Pulse duration, SCL high	0.6		ns
Slave Standard Mode					
I1	t _{w(SCLL)}	Pulse duration, SCL low	4.7		ns
I2	t _{w(SCLH)}	Pulse duration, SCL high	4		ns

- (1) The capacitive load is:
100 pF in HS mode (3.4 Mbps)
400 pF in fast-speed mode (400 Kbps)
400 pF in standard mode (100 Kbps)
- (2) SDA is equal to I2C.SR.SDA or I2C.CNTL.SDA
SCL is equal to I2C.SR.SCL or I2C.CNTL.SCL
- (3) Min = Minimum value
(4) Max = Maximum value

12.4 Audio Interface: TDM/I2S Protocol

The TPS65920/TPS65930 device acts as a master for the TDM and I2S interfaces or as a slave for only the I2S interface. If the TPS65920/TPS65930 device is the master, it must provide the frame synchronization (TDM/I2S_SYNC) and bit clock (TDM/I2S_CLK) to the host processor. If it is the slave, the TPS65920/TPS65930 device receives frame synchronization and the bit clock.

The TPS65920/TPS65930 device supports the I2S, TDM, left-justified, and right-justified data formats, but does not support TDM slave mode.

12.4.1 I2S Right- and Left-Justified Data Format

Table 12-5 and Table 12-6 assume testing over the recommended operating conditions (see Figure 12-2 and Figure 12-3).

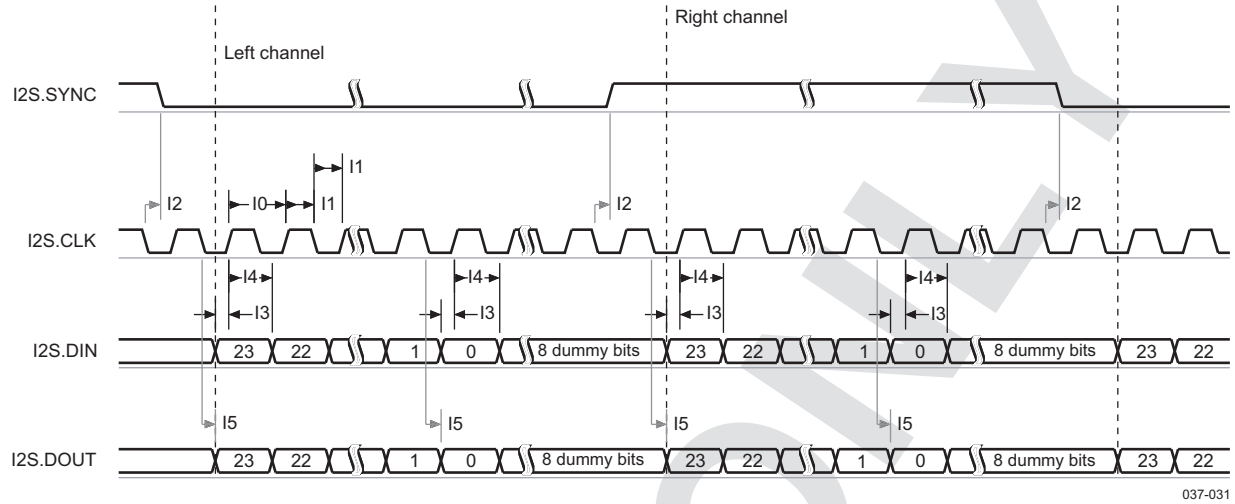


Figure 12-2. I2S Interface—I2S Master Model

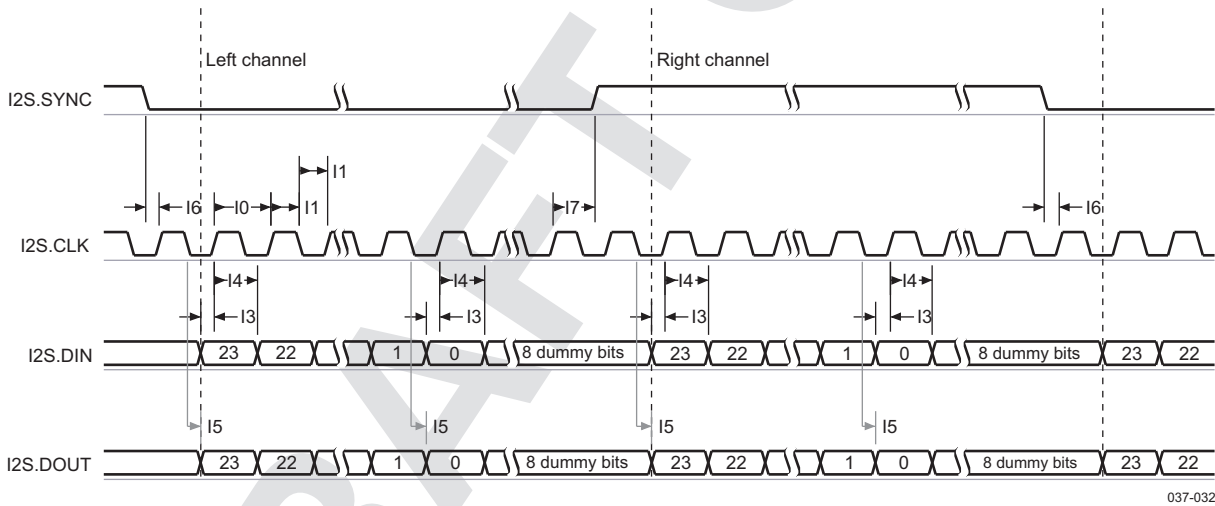


Figure 12-3. I2S Interface—I2S Slave Mode

The timing requirements listed in Table 12-5 are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is $t_R/t_F = 1.0 \text{ ns}/6.5 \text{ ns}$
- Capacitance load range of outputs (CLK, SYNC, DOUT) is $C_{\text{Load}} = 1 \text{ pF}/30 \text{ pF}$

The input timing requirements in [Table 12-5](#) are given by considering a rising or falling time of 6.5 ns.

Table 12-5. I2S Interface—Timing Requirements

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
Master Mode					
I3	t _{su} (DIN-CLKH)	Setup time, I2S.DIN valid to I2S.CLK high ²	25		ns
I4	t _h (DIN-CLKH)	Hold time, I2S.DIN valid from I2S.CLK high.	0		ns
Slave Mode					
I0	t _c (CLK)	Cycle time, I2S.CLK ⁽³⁾	1/64 * F _s		ns
I1	t _w (CLK)	Pulse duration, I2S.CLK high or low ⁽⁴⁾	0.45 * P	0.55 * P	ns
I3	t _{su} (DIN-CLKH)	Setup time, I2S.DIN valid to I2S.CLK high	5		ns
I4	t _h (DIN-CLKH)	Hold time, I2S.DIN valid from I2S.CLK high.	5		ns
I6	t _{su} (SYNC-CLKH)	Setup time, I2S.SYNC valid to I2S.CLK high	5		ns
I7	t _h (SYNC-CLKH)	Hold time, I2S.SYNC valid from I2S.CLK high	5		ns

(1) Min = Minimum value

(2) Max = Maximum value

(3) F_s = 8 to 48 kHz; 96 kHz for RX path only

(4) P = I2S.CLK period

The capacitive load for [Table 12-6](#) is 7 pF. [Table 12-6](#) lists the switching characteristics for the I2S interface.

Table 12-6. I2S Interface—Switching Characteristics

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
Master Mode					
I0	t _c (CLK)	Cycle time, I2S.CLK ⁽³⁾	1/64 * F _s		ns
I1	t _w (CLK)	Pulse duration, I2S.CLK high or low ⁽⁴⁾	0.45 * P	0.55 * P	ns
I2	t _d (CLKL-SYNC)	Delay time, I2S.CLK falling edge to I2S.SYNC transition	−10	10	ns
I5	t _d (CLKL-DOUT)	Delay time, I2S.CLK falling edge to I2S.DOUT transition	−10	10	ns
Slave Mode					
I5	t _d (CLKL-DOUT)	Delay time, I2S.CLK falling edge to I2S.DOUT transition	0	20	ns

(1) Min = Minimum value

(2) Max = Maximum value

(3) F_s = 8 to 48 kHz; 96 kHz for RX path only

(4) P = I2S.CLK period

12.4.2 TDM Data Format

Table 12-7 and Table 12-8 assume testing over the recommended operating conditions (see Figure 12-4).

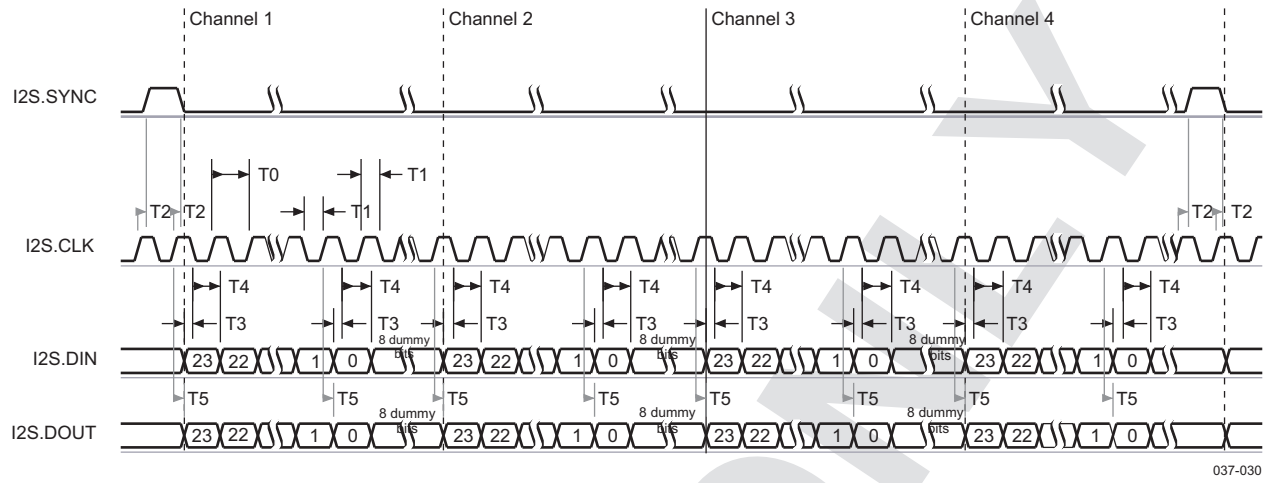


Figure 12-4. TDM Interface—TDM Master Mode

The timing requirements listed in [Table 12-7](#) are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is $t_R/t_F = 1.0 \text{ ns}/6.5 \text{ ns}$
- Capacitance load range of outputs (CLK, SYNC, DOUT) is $C_{\text{Load}} = 1 \text{ pF}/30 \text{ pF}$

Table 12-7. TDM Interface Master Mode—Timing Requirements

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
T3	$t_{\text{su}}(\text{DIN-CLKH})$	Setup time, TDM.DIN valid to TDM.CLK high	25		ns
T4	$t_{\text{h}}(\text{DIN-CLKH})$	Hold time, TDM.DIN valid from TDM.CLK high	0		ns

(1) Min = Minimum value

(2) Max = Maximum value

[Table 12-8](#) lists the switching characteristics of the TDM interface master mode.

Table 12-8. TDM Interface Master Mode—Switching Characteristics

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
T0	$t_{\text{c}}(\text{CLK})$	Cycle time, TDM.CLK ⁽³⁾	$1/64 * F_s$		ns
T1	$t_{\text{w}}(\text{CLK})$	Pulse duration, TDM.CLK high or low ⁽⁴⁾	$0.45 * P$	$0.55 * P$	ns
T2	$t_{\text{d}}(\text{CLKL-SYNC})$	Delay time, TDM.CLK rising edge to TDM.SYNC transition	–10	10	ns
T5	$t_{\text{d}}(\text{CLKL-DOUT})$	Delay time, TDM.CLK rising edge to TDM.DOUT transition	–10	12	ns

(1) Min = Minimum value

(2) Max = Maximum value

(3) $F_s = 8$ to 48 kHz ; 96 kHz for RX path only

(4) $P = \text{TDM.CLK period}$

12.5 JTAG Interfaces

The TPS65920/TPS65930 device JTAG TAP controller handles standard IEEE JTAG interfaces. This section describes the timing requirements for the tools used to test TPS65920/TPS65930 device power management.

The JTAG/TAP module provides a JTAG interface according to IEEE Std1149.1a. This interface uses the four I/O pins TMS, TCK, TDI, and TDO. The TMS, TCK, and TDI inputs contain a pullup device, which makes their state high when they are not driven. The output TDO is a 3-state output, which is high impedance except when data are shifted between TDI and TDO.

- TCK is the test clock signal.
- TMS is the test mode select signal.
- TDI is the scan path input.
- TDO is the scan path output.

TMS and TDO are multiplexed at the top level with the GPIO0 and GPIO1 pins. The dedicated external TEST pin switches from functional mode (GPIO0/GPIO1) to JTAG mode (TMS/TDO). The JTAG operations are controlled by a state-machine that follows the IEEE Std1149.1a state diagram. This state-machine is reset by the TPS65920/TPS65930 internal power-on reset (POR). A test mode is selected by writing a 6-bit word (instruction) into the instruction register and then accessing the related data register.

[Table 12-9](#) and [Table 12-10](#) assume testing over the recommended operating conditions (see [Figure 12-5](#)).

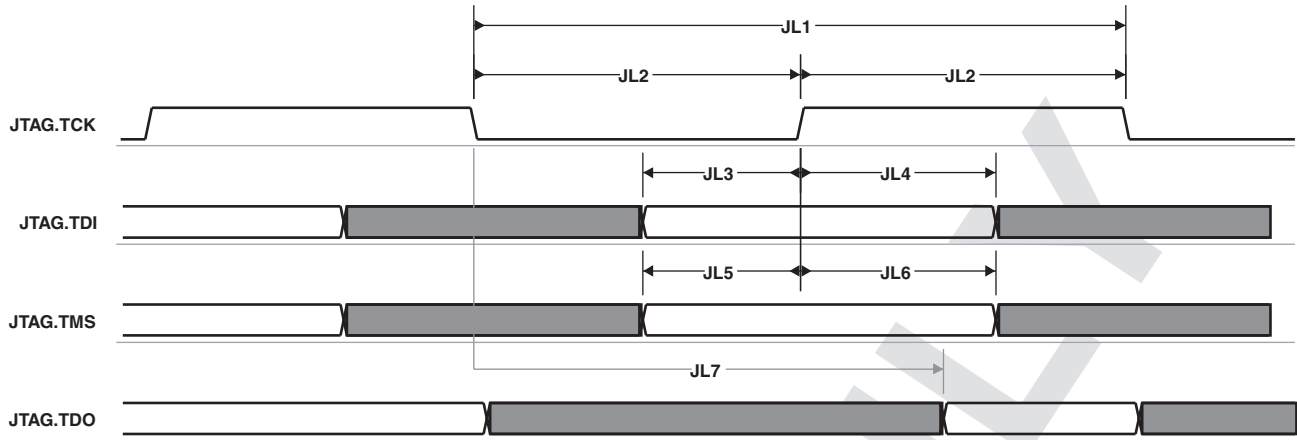


Figure 12-5. JTAG Interface Timing

The input timing requirements are given by considering a rising or falling edge of 7 ns.

Table 12-9. JTAG Interface—Timing Requirements

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
Clock					
JL1	t _c (TCK)	Cycle time, JTAG.TCK period	30		ns
JL2	t _w (TCK)	Pulse duration, JTAG.TCK high or low ⁽³⁾	0.48*P	0.52*P	ns
Read Timing					
JL3	t _{su} (TDIV-TCKH)	Setup time, JTAG.TDI valid before JTAG.TCK high	8		ns
JL4	t _h (TDIV-TCKH)	Hold time, JTAG.TDI valid after JTAG.TCK high	5		ns
JL5	t _{su} (TMSV-TCKH)	Setup time, JTAG.TMS valid before JTAG.TCK high	8		ns
JL6	t _h (TMSV-TCKH)	Hold time, JTAG.TMS valid after JTAG.TCK high	5		ns

(1) Min = Minimum value

(2) Typ = Typical value

(3) P = JTAG.TCK clock period

The capacitive load is 35 pF.

Table 12-10. JTAG Interface—Switching Characteristics

Notation	Parameter		Min ⁽¹⁾	Max ⁽²⁾	Unit
Write Timing					
JL7	t _{d(TCK-TDOV)}	Delay time, JTAG, TCK active edge to JTAG.TDO valid	0	14	ns

(1) Min = Minimum value

(2) Max = Maximum value

13 Debouncing Time

Table 13-1 lists the characteristics of debouncing.

Table 13-1. Debouncing

Debouncing Functions	Block	Programmable	Debouncing Time	Default
USB plug detection	USB	No	9x50 ms	9x50 ms
Plug/unplug detection VBUS ⁽¹⁾	USB	Yes	0 to 250 ms (32/32468-second steps)	28 ms
Plug/unplug detection ID ⁽²⁾	USB	Yes	0 to 250 ms (32/32468-second steps)	50 ms
Debouncing function interrupt generation debounce for VBUS and ID ⁽³⁾	Power	Yes	0 to 250 ms	30 ms
Hot-die detection	Thermistor	No	60 μ s	60 μ s
Thermal shutdown detection		No	60 μ s	60 μ s
PWRON ⁽⁴⁾	Start/stop button	No	31.25 ms	31.25 ms
NRESWARM	Button reset	No	60 μ s	60 μ s
SIM card plug/unplug	GPIO	Yes	0 or 30 ms \pm 1 ms	0 ms
MMC1 (plug/unplug)	GPIO	Yes	0 or 30 ms \pm 1 ms	0 ms

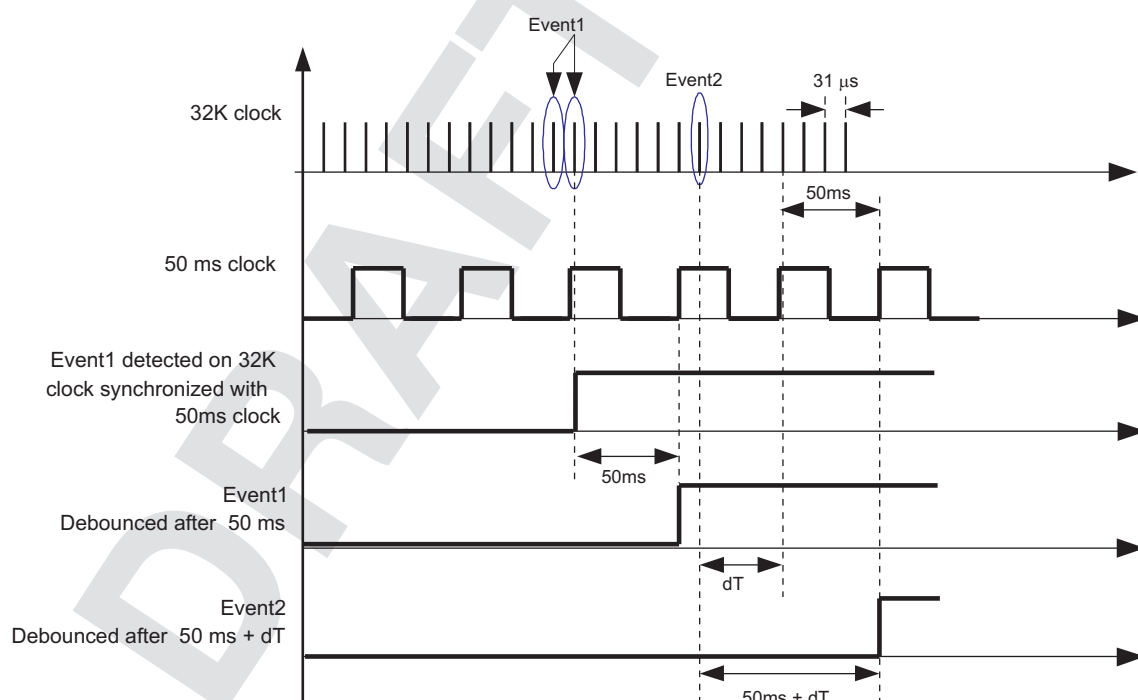
(1) Programmable in the VBUS_DEBOUNCE register

(2) Programmable in the ID_DEBOUNCE register

(3) Programmable in the RESERVED_E[2:0] CFG_VBUSDEB register

(4) The PWRON signal is debounced 1024*CLK32K (maximum 1026*CLK32K) falling edge in master mode.

Figure 13-1 is a sample debouncing sequence chronogram.



037-029

Figure 13-1. Debouncing Sequence Chronogram Example

Event1 is correctly debounced after 50ms. Event2 is debounced after 50ms + dT because the capture of the event is considered after the next rising edge of the 50-ms clock.

14 External Components

Table 14-1 lists the TPS65920/TPS65930 device external components.

Table 14-1. TPS65920/TPS65930 External Components

Function	Component	Reference	Value	Note	Link
Power Supplies					
VDD1	Capacitor	C _{VDD1.IN}	10 μ F	Range \pm 50% ESR min = 1 m Ω ESR max = 20 m Ω Taiyo Yuden: JMK212BJ106KD	Figure 4-1
	Capacitor	C _{VDD1.OUT}	10 μ F	Range \pm 50% ESR min = 1 m Ω ESR max = 20 m Ω Taiyo Yuden: JMK212BJ106KD	
	Inductor	L _{VDD1}	1 μ H	Range \pm 30% DCR max = 100 m Ω	
VDD2	Capacitor	C _{VDD2.IN}	10 μ F	Range \pm 50% ESR min = 1 m Ω ESR max = 20 m Ω Taiyo Yuden: JMK212BJ106KD	Figure 4-1
	Capacitor	C _{VDD2.OUT}	10 μ F	Range \pm 50% ESR min = 1 m Ω ESR max = 20 m Ω Taiyo Yuden: JMK212BJ106KD	
	Inductor	L _{VDD2}	1 μ H	Range \pm 30% DCR max = 100 m Ω	
VIO	Capacitor	C _{VIO.IN}	10 μ F	Range \pm 50% ESR min = 1 m Ω ESR max = 20 m Ω Taiyo Yuden: JMK212BJ106KD	Figure 4-1
	Capacitor	C _{VIO.OUT}	10 μ F	Range \pm 50% ESR min = 1 m Ω ESR max = 20 m Ω Taiyo Yuden: JMK212BJ106KD	
	Inductor	L _{VIO}	1 μ H	Range \pm 30% DCR max = 100 m Ω	
VRUSB_3V	Capacitor	C _{VUSB.3P1}	1 μ F	Range: 0.3 to 2.7 μ F ESR min = 20 m Ω ESR max = 300 m Ω	Figure 4-1 Figure 7-2
VRUSB_1V5	Capacitor	C _{VINTUSB1P5.OUT}	1 μ F	Range: 0.3 to 2.7 μ F ESR min = 20 m Ω ESR max = 600 m Ω	Figure 4-1 Figure 7-2
VRUSB_1V8	Capacitor	C _{VINTUSB1P8.OUT}	1 μ F	Range: 0.3 to 2.7 μ F ESR min = 20 m Ω ESR max = 600 m Ω	Figure 4-1 Figure 7-2
VDAC	Capacitor	C _{VDAC.IN}	1 μ F	Range: 0.3 to 2.7 μ F ESR min = 20 m Ω ESR max = 600 m Ω	Figure 4-1
	Capacitor	C _{VDAC.OUT}	1 μ F	Range: 0.3 to 2.7 μ F ESR min = 20 m Ω ESR max = 600 m Ω	
VPLLA3R	Capacitor	C _{VPLLA3R.IN}	1 μ F	Range: 0.3 to 2.7 μ F ESR min = 20 m Ω ESR max = 600 m Ω	Figure 4-1
VPLL1	Capacitor	C _{VPLL1.OUT}	1 μ F	Range: 0.3 to 2.7 μ F ESR min = 20 m Ω ESR max = 600 m Ω	Figure 4-1

Table 14-1. TPS65920/TPS65930 External Components (continued)

Function	Component	Reference	Value	Note	Link
VMMC1	Capacitor	C _{VMMC1.IN}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 4-1
	Capacitor	C _{VMMC1.OUT}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	
VAUX12S	Capacitor	C _{VAUX12S.IN}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 4-1
VAUX2	Capacitor	C _{VAUX2.OUT}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 4-1
VINT	Capacitor	C _{VINT.IN}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 4-1
VINTANA1	Capacitor	C _{VINTANA1.OUT}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 4-1
VINTANA2	Capacitor	C _{VINTANA2.OUT}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 4-1
VINTDIG	Capacitor	C _{VINTDIG.OUT}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 4-1
VBAT.USB	Capacitor	C _{VBAT.USB}	1 μF	Range: 0.3 to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 7-2
USB CP	Capacitor	C _{VBUS.FC}	2.2 μF ± 40%	ESR max = 20 mΩ	Figure 7-2
	Capacitor	C _{VBUS.IN}	10 μF		
	Capacitor	C _{VBUS}	4.7 μF ± 40%	ESR max = 20 mΩ	
32.768 kHz					
32K OSC	Capacitor	C _{XIN}	10 pF	Range: 9 pF to 12.5 pF	Figure 11-5
	Capacitor	C _{XOUT}	10 pF		
	Quartz	X _{32.768kHz}	32.768 kHz	±30 ppm (at 25°C) ±200 ppm (–40°C to 85°C)	
Audio					
External class-D predriver left	Capacitor	C _{PL.O}	50 pF		Figure 6-2
	Capacitor	C _{PL}	1 μF		
	Resistor	R _{PL}	>15 kΩ		
	Resistor	R _{PL.M}	>15 kΩ		
	Resistor	R _{PL.O}	10 kΩ		
	Capacitor	C _{PL.M}	1 μF		
External class-D predriver right	Capacitor	C _{PR.O}	50 pF		Figure 6-2
	Capacitor	C _{PR}	1 μF		
	Resistor	R _{PR}	>15 kΩ		
	Resistor	R _{PR.M}	>15 kΩ		
	Resistor	R _{PR.O}	10 kΩ		
	Capacitor	C _{PR.M}	1 μF		
Vibrator H-bridge	Ferrite bead	L _{V.M}		BLM18BD221S1N	Figure 6-3
	Ferrite bead	L _{V.P}		BLM18BD221S1N	
	Capacitor	C _{V.V}	1 μF		
	Capacitor	C _{V.M}	1 nF		
	Capacitor	C _{V.P}	1 nF		

Table 14-1. TPS65920/TPS65930 External Components (continued)

Function	Component	Reference	Value	Note	Link
MIC main (pseudo differential mode)	Capacitor	C _{MM.M}	100 nF		Figure 6-6
	Capacitor	C _{MM.P}	100 nF		
	Capacitor	C _{MM.O}	47 pF		
	Resistor	R _{MM.O}	−500 Ω		
	Resistor	R _{MM.MP}	−1.7 kΩ		
	Capacitor	C _{MM.B}	0 to 200 pF	If greater than 200 pF, a serial resistor is required for bias stability	
MIC main (differential mode)	Capacitor	C _{MM.M}	100 nF		Figure 6-7
	Capacitor	C _{MM.P}	100 nF		
	Capacitor	C _{MM.PM}	47 pF		
	Capacitor	C _{MM.O}	47 pF		
	Capacitor	C _{MM.GM}	47 pF		
	Capacitor	C _{MM.GP}	47 pF		
	Resistor	R _{MM.BP}	1 kΩ		
	Resistor	R _{MM.GM}	1 kΩ		
	Capacitor	C _{MM.B}	0 to 200 pF	If greater than 200 pF, a serial resistor is required for bias stability	
VMIC1	Capacitor	C _{VMIC1.OUT}	1 μF	Range: 0.3 μF to 3.3 μF ESR min = 20 mΩ ESR max = 600 mΩ	
Silicon MIC	Capacitor	C _{SM}	1 μF		Figure 6-8
	Capacitor	C _{SM.P}	100 nF		
	Capacitor	C _{SM.M}	100 nF		
	Capacitor	C _{SM.PG}	47 nF		
	Resistor	R _{SM}	>500 Ω		
Auxiliary right	Capacitor	C _{AUXR}	100 nF		Figure 6-9
	Capacitor	C _{AUXR.M}	47 pF		
LED Driver					
LED	Resistor	R _{LED.A}	120 Ω	Needed for each LED	Figure 9-1
	Resistor	R _{LED.B}	160 kΩ	Needed for each LED	
I ² C Bus—External Pullup					
I ² C SmartReflex	Resistor	R _{PSR.SDA}	Pullups for various bus capacitances (C _L) and I ² C speeds (Std, Fast, and HS) If C _L = 10 pF: Std = 118 kΩ, Fast = 35.4 kΩ, HS = 4.7 kΩ If C _L = 12 pF: Std = 98.3 kΩ, Fast = 29.5 kΩ, HS = 3.9 kΩ If C _L = 50 pF: Std = 23.6 kΩ, Fast = 7.1 kΩ, HS = 940 Ω If C _L = 100 pF: Std = 11.8 kΩ, Fast = 3.54 kΩ, HS = 470 Ω If C _L ≤ 12 pF, there is no need for an external pullup, the internal 3-kΩ pullup can be used. If an external pullup is used, disable the internal 3-kΩ pullup (reference the GPPUPDCTR1 register; see the TRM).		Section 12.3
	Resistor	R _{PSR.SCL}			
I ² C control	Resistor	R _{CNTL.SD;}			
	Resistor	R _{CNTL.SCL}			

15 TPS65920/TPS65930 Package

15.1 TPS65920/TPS65930 Standard Package Symbols

Figure 15-1 shows the printed device reference.

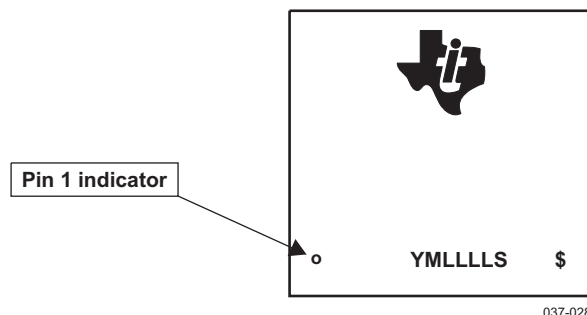


Figure 15-1. Printed Device Reference

Table 15-1 lists the fields and their meanings.

Table 15-1. TPS65920/TPS65930 Nomenclature Description

Field	Meaning
P	Marking used to note prototype (X), preproduction (P), or qualified/production device (blank) ⁽¹⁾
A	Mask set version descriptor (initial silicon = BLANK, first silicon revision = A, second silicon revision = B,...) ⁽²⁾
YM	Year month
LLLLS	Lot code
\$	Fab planning code

(1) A blank in the symbol or part number is collapsed so there are no gaps between characters.

(2) Initial silicon version is ES1.0; first revision can be named ES2.0, ES1.1, or ES1.01, depending on the level of change.
Note: The device name is a maximum of 10 characters.

15.2 Package Thermal Resistance Characteristics

Table 15-2 and Table 15-3 list the thermal resistance characteristics for the TPS65920 and TPS65930 devices, respectively.

Table 15-2. TPS65920 Thermal Resistance Characteristics

$R_{\theta JA}$ (°C/W)	$R_{\theta JB}$ (°C/W)	$R_{\theta JC}$ (°C/W)	Board Type
33.40	13.80	6.74 ⁽¹⁾	2S2P ⁽²⁾
57.04	14.50	6.74 ⁽¹⁾	1S0P ⁽²⁾

(1) This measurement is not affected by the board on which the device is mounted.

(2) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements).

Table 15-3. TPS65930 Thermal Resistance Characteristics

$R_{\theta JA}$ (°C/W)	$R_{\theta JB}$ (°C/W)	$R_{\theta JC}$ (°C/W)	Board Type
33.42	13.81	6.74 ⁽¹⁾	2S2P ⁽²⁾
57.05	14.51	6.74 ⁽¹⁾	1S0P ⁽²⁾

(1) This measurement is not affected by the board on which the device is mounted.

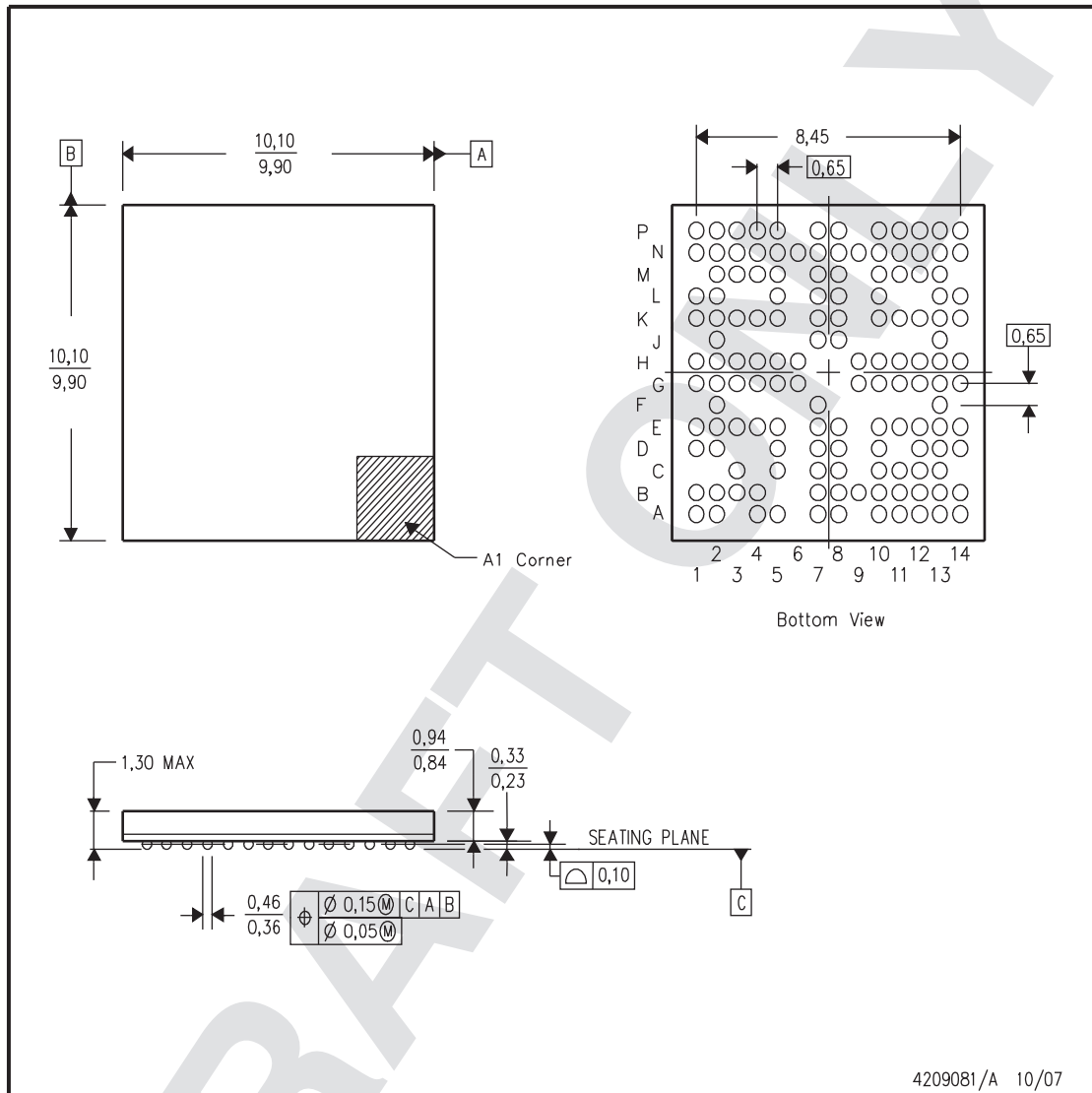
(2) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements).

15.3 Mechanical Data

Figure 15-2 shows the TPS65920/TPS65930 mechanical package.

ZCH (S-PBGA-N139)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. nFBGA configuration
 - D. This is a lead-free solder ball design.

037-015

Figure 15-2. TPS65920/TPS65930 Mechanical Package

Figure 15-3 is the bottom view of the TPS65920/TPS65930 mechanical package.

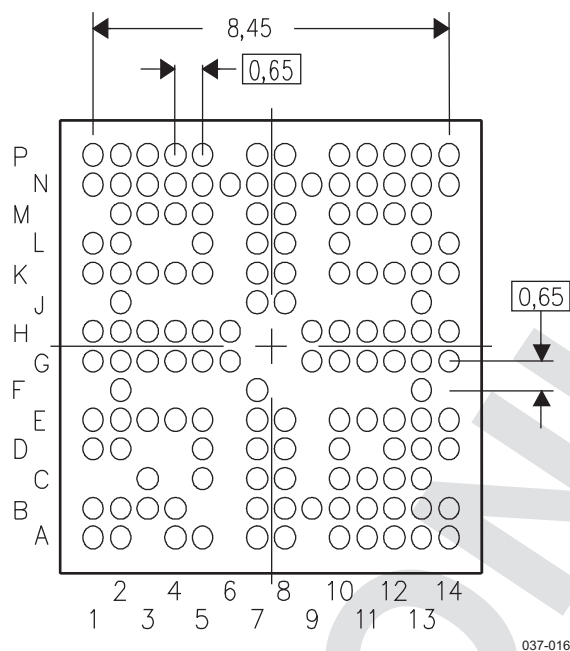


Figure 15-3. TPS65920/TPS65930 Mechanical Package Bottom View

Figure 15-4 shows the ball size.

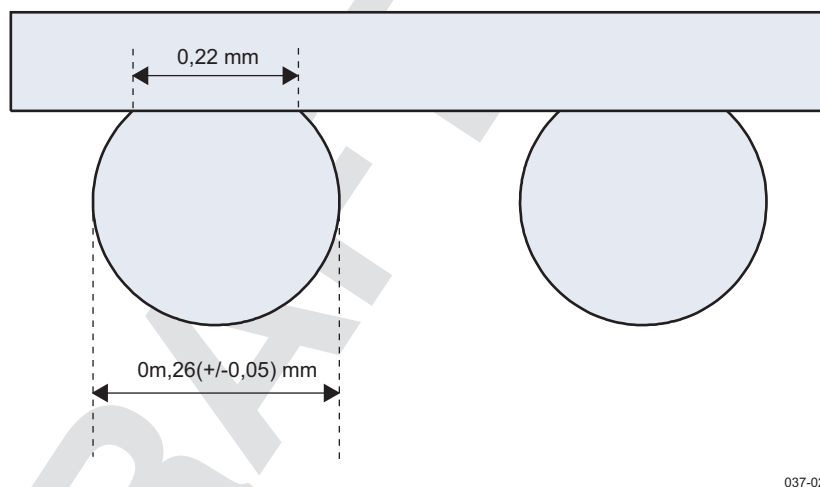


Figure 15-4. Ball Size

16 Glossary

ADC	Analog-to-digital converter
ALC	Automatic level control
ASIC	Application-specific integrated circuit
BGA	Ball grid array
BW	Signal bandwidth
CMOS	Complementary metal oxide semiconductor
CMT	Cellular mobile telephone
CPU	Central processing unit
DAC	Digital-to-analog converter
DBB	Digital baseband
DCR	Data capture record
DM	Data manual
DSP	Digital signal processor
DVFS	Dynamic voltage and frequency scaling
ESD	Electrostatic discharge
ESR	Equivalent series resistance
FS	Full speed
FSR	Full-scale range
GND	Ground
GP	General-purpose
FET	Field effect transistor
GPIO	General-purpose input/output
hiZ	High impedance
HS	High speed or high security
HW	Hardware
I ² C	Inter-integrated circuit
I2S	Inter IC sound
IC	Integrated circuit
ICN	Idle channel noise
ID	Identification
IDDQ	Direct drain quiescent current
IF	Interface
IO or I/O	Input/output
JTAG	Joint Test Action Group, IEEE 1149.1 standard
LED	Light-emitting diode
LDO	Low-dropout regulator
LJF	Left-justified format
LS	Low speed
MADC	Monitoring analog-to-digital converter

TPS65930/TPS65920
**Integrated Power Management/
Audio Codec (TPS65930 Only)**

SWCS037A–MAY 2008–REVISED SEPTEMBER 2008

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MMC	Multimedia card
NA, N/A	Not applicable
NRZI	Nonreturn to zero inverted
OCP	Open-core protocol
OTG	On-the-Go
PBGA	Plastic ball grid array
PCB	Printed circuit board
PD	Pulldown
PDM	Pulse density modulated
PFM	Pulse frequency modulation
PLL	Phase-locked loop
POL	Polarity
POR	Power-on reset
PSR	Power-supply rejection
PSRR	Power-supply rejection ratio
PU	Pullup
PWL	Pulse-width length
PWT	Pulse-width time
PWM	Pulse-width modulation
RJF	Right-justified format
RTC	Real-time clock
RX	Receive
SDI	Serial display interface
SMPS	Switch-mode power supplies
SNR	Signal-to-noise ratio
SW	Software
SYNC/SYNCHRO	Synchronization
SYS	System
TBD	To be defined
THRU	Feed through
TRM	Technical reference manual
TX	Transmit
UART	Universal asynchronous receiver/transmitter
ULPI	UTMI+ low pin Interface
UPR	Uninterrupted power rail
USB	Universal serial bus
UTMI	USB transceiver macrocell Interface

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